Display Elektronik GmbH

DATA SHEET

E-Paper Display

DEE 400300A2 – W

4,2"
E-PAPER DISPLAY

Product Specification   **Ver.: 0**

16.03.2017

Specification For OED 4.2″ E-Paper

Model NO.: DEE 400300A2-W

Prepared by	Checked by	Approved by

Customer approval

Customer	Approved by	Date of approval

Version	**Content**	**Date**	**Producer**
0	New Release	16.03.2017	MH

CONTENTS

1 General Description

DEE 400300A2-W is an Active Matrix Electrophoretic Display(AM EPD), with interface and a reference system design. The 4.2" active area contains 400x300 pixels. The module is a TFT-array driving electrophoretic display, with integrated circuits including gate buffer, source buffer, MCU interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2 Features

◆ 400×300 Pixels Display
◆ White Reflectance above 30%
◆ Contrast Ratio above 8:1
◆ Ultra Wide Viewing Angle
◆ Ultra Low Power Consumption
◆ Pure Reflective Mode
◆ Bi-stable Display
◆ Commercial Temperature Range
◆ Landscape, Portrait Modes
◆ Hard-Coat Antiglare Display Surface
◆ Ultra Low Current Deep Sleep Mode
◆ On Chip Display RAM
◆ Waveform stored in On-Chip OTP
◆ Serial Peripheral Interface available
◆ On-Chip Oscillator
◆ On-Chip Booster and Regulator Control for generating VCOM, Gate and Source Driving Voltage
◆ I^2C Signal Master Interface to read External Temperature Sensor

3 Application

Electronic Shelf Label System

4 Mechanical Specification

4.1 Dimension

Parameter	Specifications	Unit	Remark
Screen Size	4.2	Inch	
Display Resolution	400(H) × 300(V)	Pixel	120DPI
Active Area	84.80 × 63.60	mm	
Pixel Pitch	0.212 × 0.212	mm	
Pixel Configuration	Square		
Outline Dimension	91.00 × 77.00 × 1.15	mm	
Weight	16.4	g	

4.2 Mechanical Drawing of EPD Module
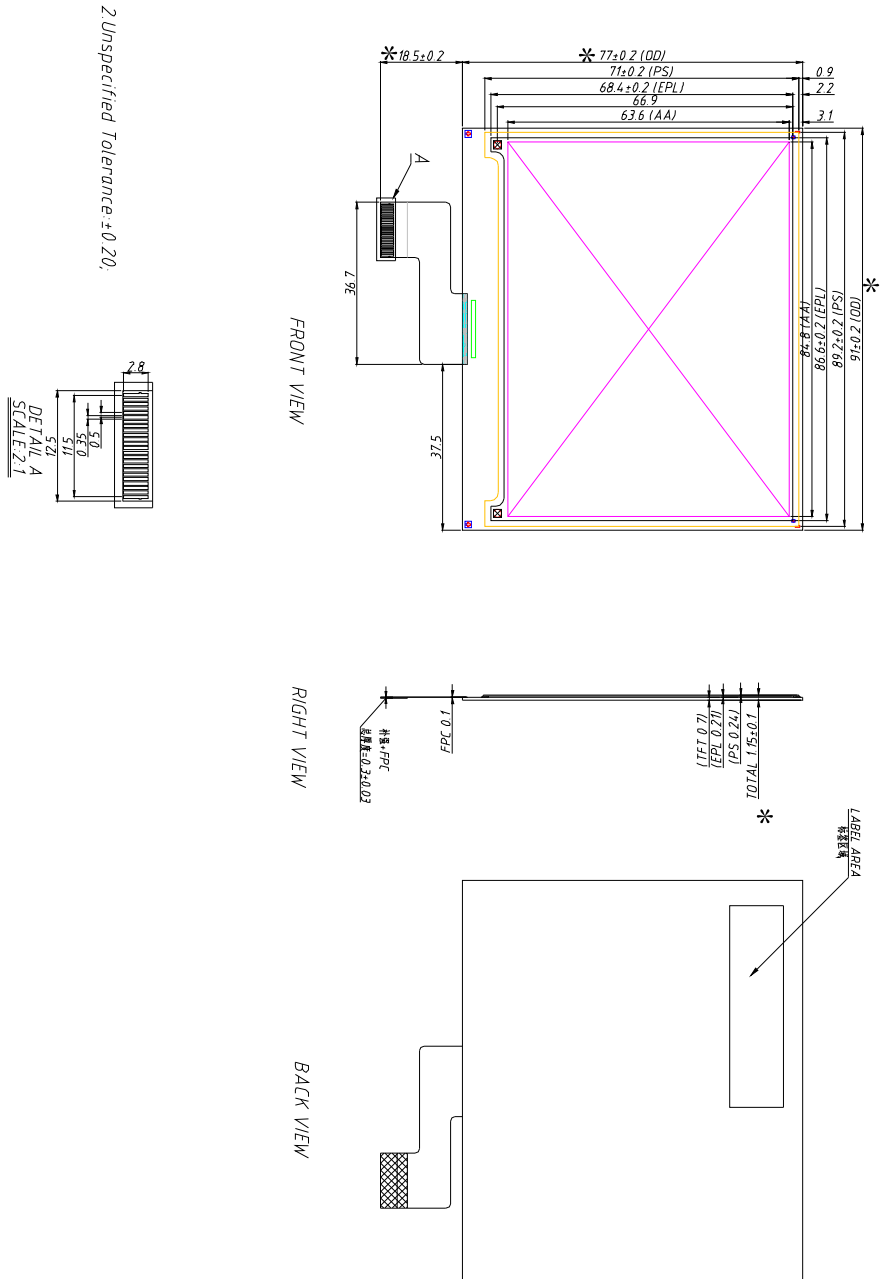
5 Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC		Do not connect with other NC pins	
5	NC		Do not connect with other NC pins	
6	TSCL	O	I^2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I^2C Interface to digital temperature sensor Data pin	
8	BS1	I	Bus Interface selection pin	Note 5-4
9	BUSY	O	Busy state output pin	Note 5-3
10	RES#	I	Reset signal input. Active Low.	
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	D0	I	Serial Clock pin (SPI)	
14	D1	I	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS under all circumstances	
19	VPP	P	Power Supply for OTP Programming	
20	VSH	C	Positive Source driving voltage	
21	VGH	C	Positive Gate driving voltage	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Negative Gate driving voltage	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/Output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at D1 will be interpreted as data. When the pin is pulled LOW, the data at D1 will be interpreted as command.

Note 5-3: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent, e.g., The chip would put Busy pin High when

- Outputting display waveform
- Programming with OTP
- Communicating with digital temperature sensor

Note 5-4: Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI)
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6 Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{CI}	-0.5 to +4.0	V
Logic Input voltage	V_{IN}	-0.5 to V_{CI} +0.5	V
Logic Output voltage	V_{OUT}	-0.5 to V_{CI} +0.5	V

Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, T_{OPR} =25℃.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Logic supply voltage	V_{CI}	-	VCI	2.4	3.0	3.7	V
High level input voltage	V_{IH}	-	-	0.8 V_{CI}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2 V_{CI}	V
High level output voltage	V_{OH}	IOH = -100uA	-	0.9 V_{CI}	-	-	V
Low level output voltage	V_{OL}	IOL = 100uA	-	-	-	0.1 V_{CI}	V
Typical power panel	P_{TYP}	-	-	-	45	240	mW
Deep sleep mode	P_{STPY}	-	-	-	0.006	-	mW
Typical operating current	Iopr_VCI	V_{CI} =3.0V	-	-	15	80	mA

Sleep mode current	Islp_VCI	VCI=3.0V DC/DC OFF No clock No output load Ram data retain	VCI	-	35	50	uA
Deep sleep mode current	Idslp_VCI	VCI=3.0V DC/DC OFF No clock No output load Ram data not retain	VCI	-	2	5	uA
Operation temperature	T_{OPR}	-	-	0	-	50	°C
Operating relative humidity	RHop	-	-	-	-	70	%RH
Storage temperature	TSTG	-	-	-20	-	70	°C
Storage relative humidity	RHst	-	-	30	-	60	%RH

Notes: 1. The typical power is measured with following transition from horizontal 2 gray scale pattern to vertical 2 gray scale pattern. (Figure 6-1)

2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by OED.
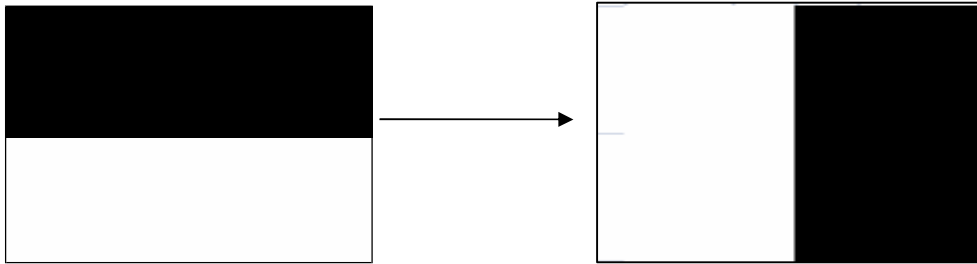

Figure 6-2 The typical power consumption measure pattern

6.3 Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VCI=3.0V, T_{OPR} =25°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	-	VCOM	-4.0	-	-0.2	V
Positive Source output voltage	V_{SH}	-	S0-399	+14.5	+15	+15.5	V
Negative Source output voltage	V_{SL}	-	S0-399	-15.5	-15	-14.5	V
Positive gate output voltage	Vgh	-	G0-G299	+21	+22	+23	V
Negative gate output voltage	Vgl	-	G0-G299	-21	-20	-19	V

6.4 MCU Interface

6.4.1 MCU Interface Selection

MCU interface consist of 2 data/command pins and 3 control pins. The pin assignment at different interface mode is summarized in Table 6-4-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Connnand Interface		Control Signal		
Bus interface	D1	D0	CS#	D/C#	RES#
4-wire SPI	SDIN	SCLK	CS#	D/C#	RES#
3-wire SPI	SDIN	SCLK	CS#	L	RES#

Table 6-4-1: MCU interface assignment under different bus interface mode

6.4.2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In 4-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN.

Function	CS#	D/C#	SCLK
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

Table 6-4-2: Control pins of 4-wire Serial interface

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.

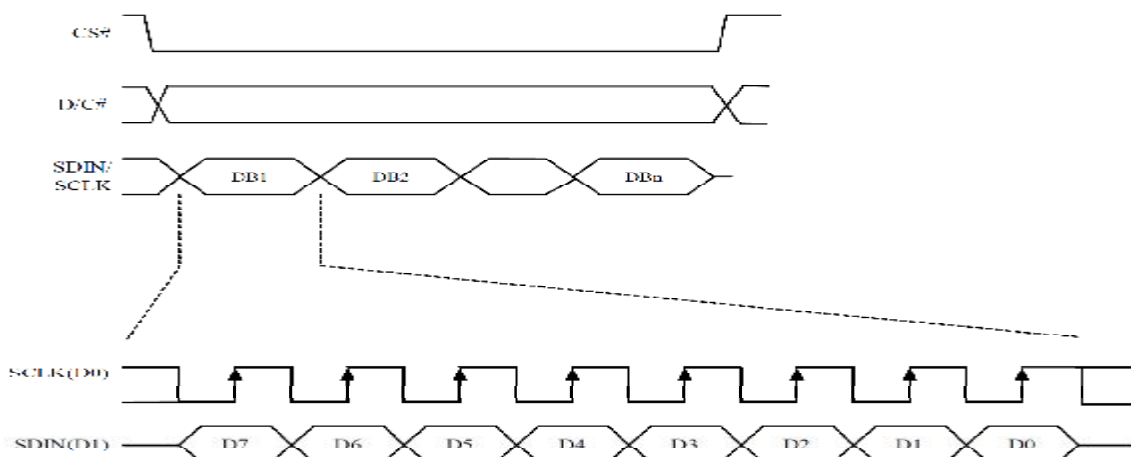Under serial mode, only write operations are allowed.

Figure 6-4-2: Write procedure in 4-wire SPI mode

6.4.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#. In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

Under serial mode, only write operations are allowed.

Function	CS#	D/C#	SCLK
Write command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

Note：↑ stands for rising edge of signal
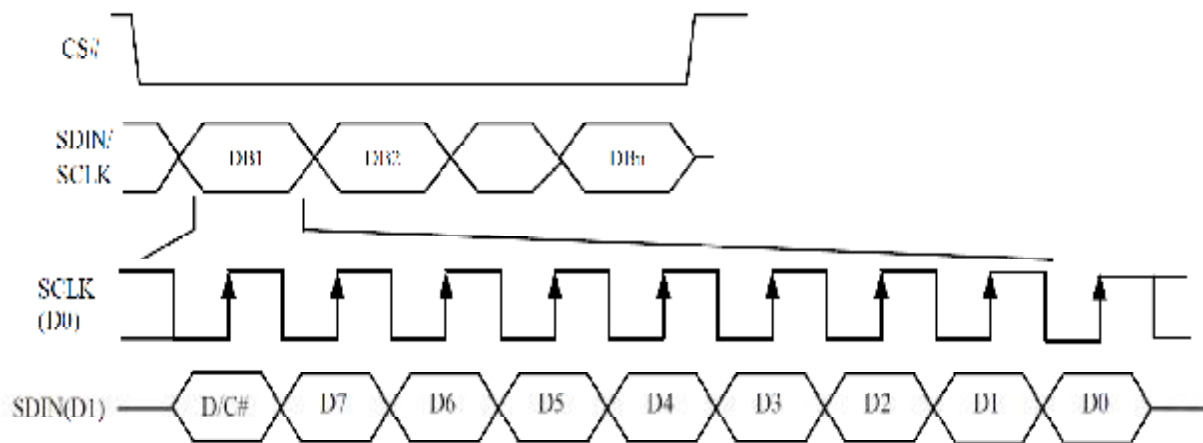
Table 6-4-3: Control pins of 3-wire Serial interface

Figure 6-4-3: Write procedure in 3-wire SPI mode

7 Optical Specification

Symbol	Parameter	Conditions	Values			Units	Notes
			Min.	Typ.	Max		
R	White Reflectivity	White	30	35	-	%	7-1
CR	Contrast Ratio		8:1	10:1	-	-	7-2
白△L 24h	Reduce		-	≤4	-	-	-
T_{update}	Image update time	at 25 ℃	-	2100	-	ms	-

Notes: 7-1. Luminance meter: Eye-One Pro Spectrophotometer.

7-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

8 Handling, Safety, and Environment Requirements

Warning
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.
Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricality and other rough environmental conditions.

9 Reliability Test

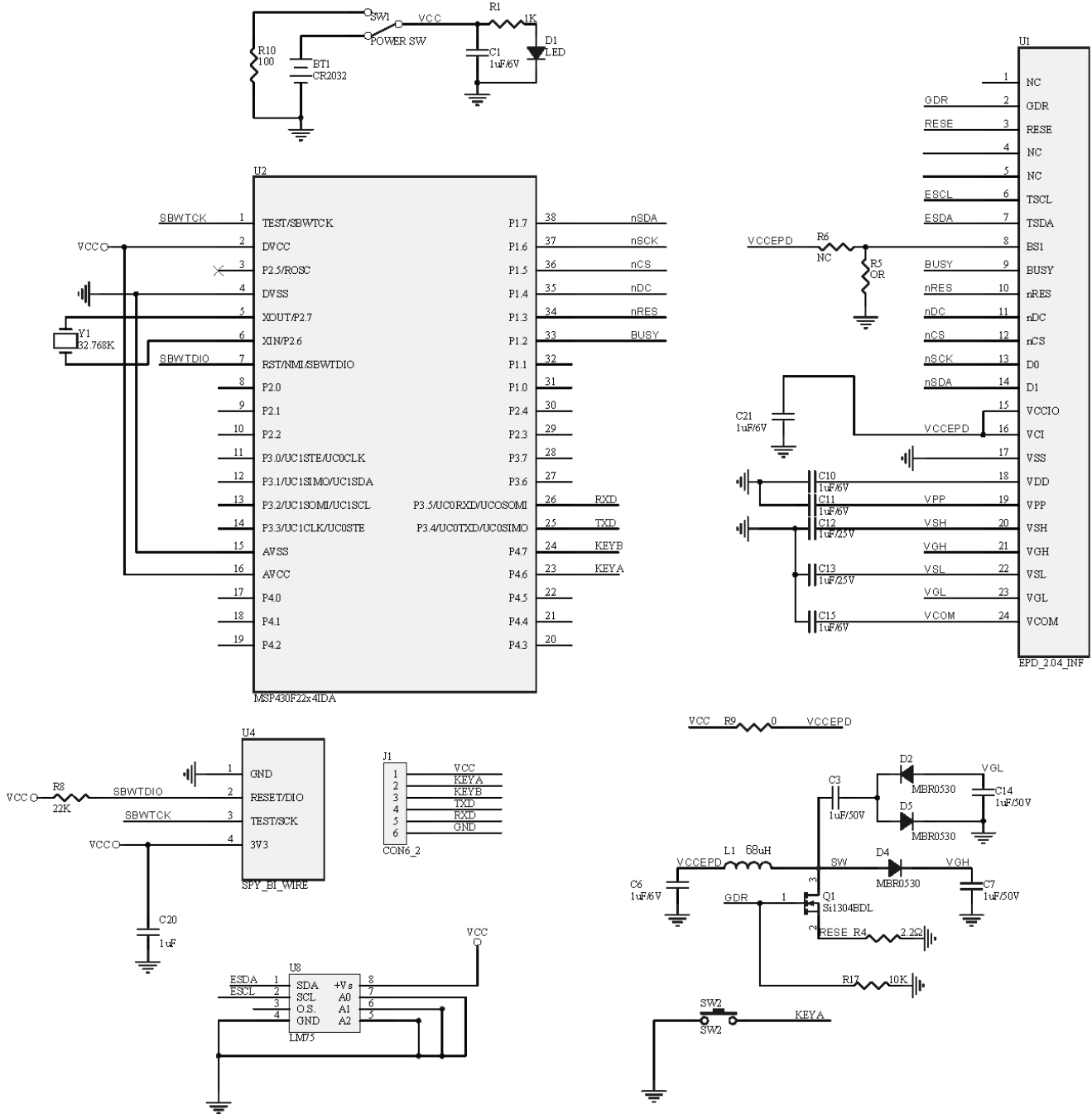| No.	Test	Condition	Method	Remark
1	High-Temperature Operation	T = +50°C, RH = 30% for 168 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
2	Low-Temperature Operation	T = 0°C for 168 hrs	IEC 60 068-2-2Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
3	High-Temperature Storage	T = +70°C, RH=23% for 168 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
4	Low-Temperature Storage	T = -25°C for 168 hrs	IEC 60 068-2-1Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
6	High Temperature, High-Humidity Storage	T = +60°C, RH=80% for 168hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
7	Thermal Shock	1 cycle:[-25°C 30min]→[+70 °C 30 min] : 50 cycles	IEC 60 068-2-14	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
8	Package Vibration	1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
9	Package Drop Impact	Drop from height of 122 cm on concrete surface. Drop sequence: 1 corner, 3edges, 6 faces One drop for each	Full packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
10	Electrostatic Effect (non-operating)	Machine model +/- 250V, 0Ω, 200pF	IEC 62179, IEC 62180	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.

10 Block Diagram
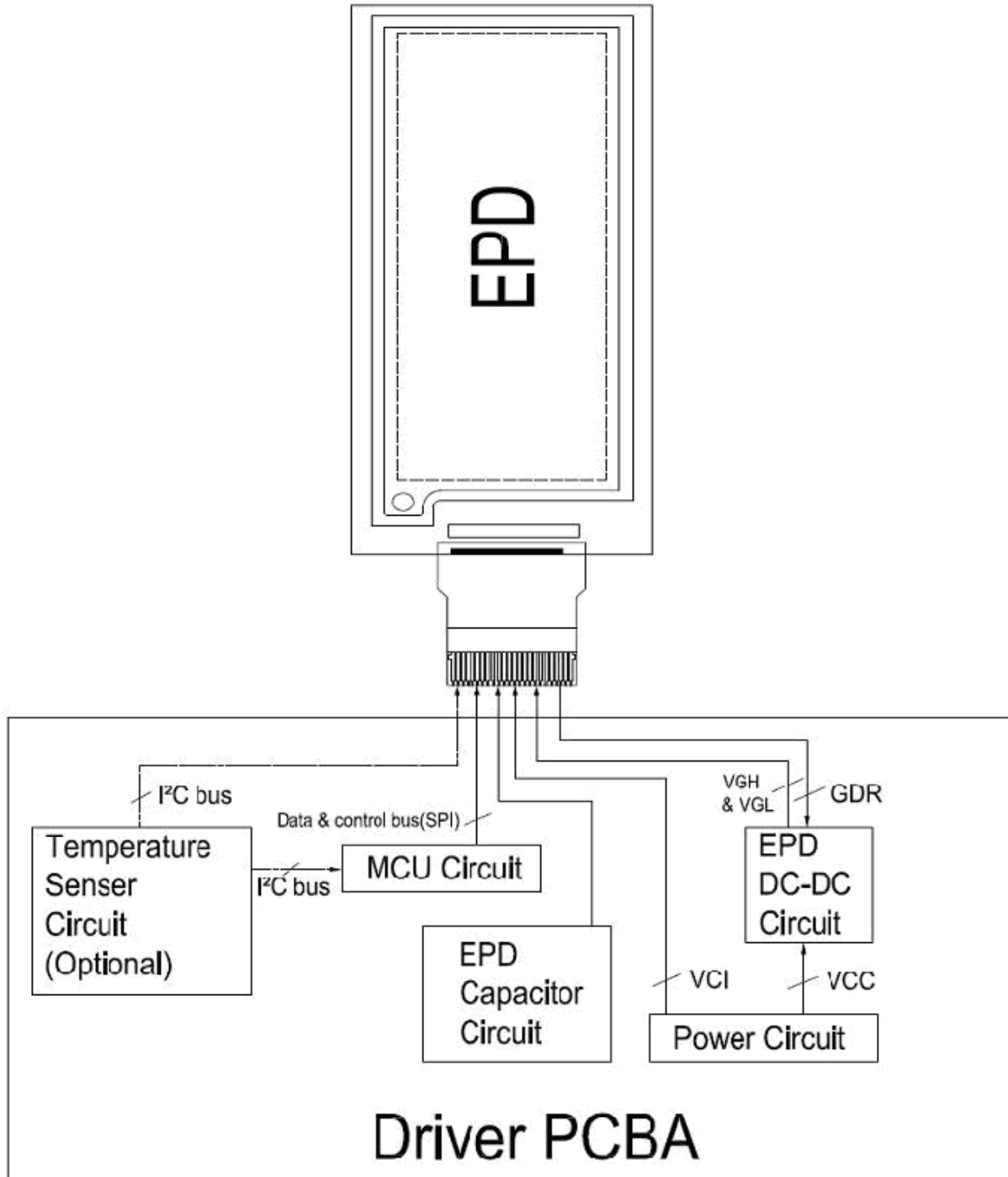
11 Typical Application Circuit with SPI Interface

Notes: 11-1. The electronic elements should be tested and verified for Max Power. We recommend the above electronic elements.