DISPLAY Elektronik GmbH

DATA SHEET

LCD MODULE

DEM 128064F1 FGH

Product Specification   *Version: 1*

27.02.2024

GENERAL SPECIFICATION

MODULE NO. :

DEM 128064F1 FGH

Version No.	Change Description	Date
0	Original Version	23.02.2024
1	Update the block diagram on page 4	27.02.2024

PREPARED BY: LM   **DATE:**27.02.2024

APPROVED BY: WHK   **DATE:**27.02.2024

CONTENTS

1. FUNCTIONS & FEATURES

- DEM 128064F1 FGH Series LCD Type :

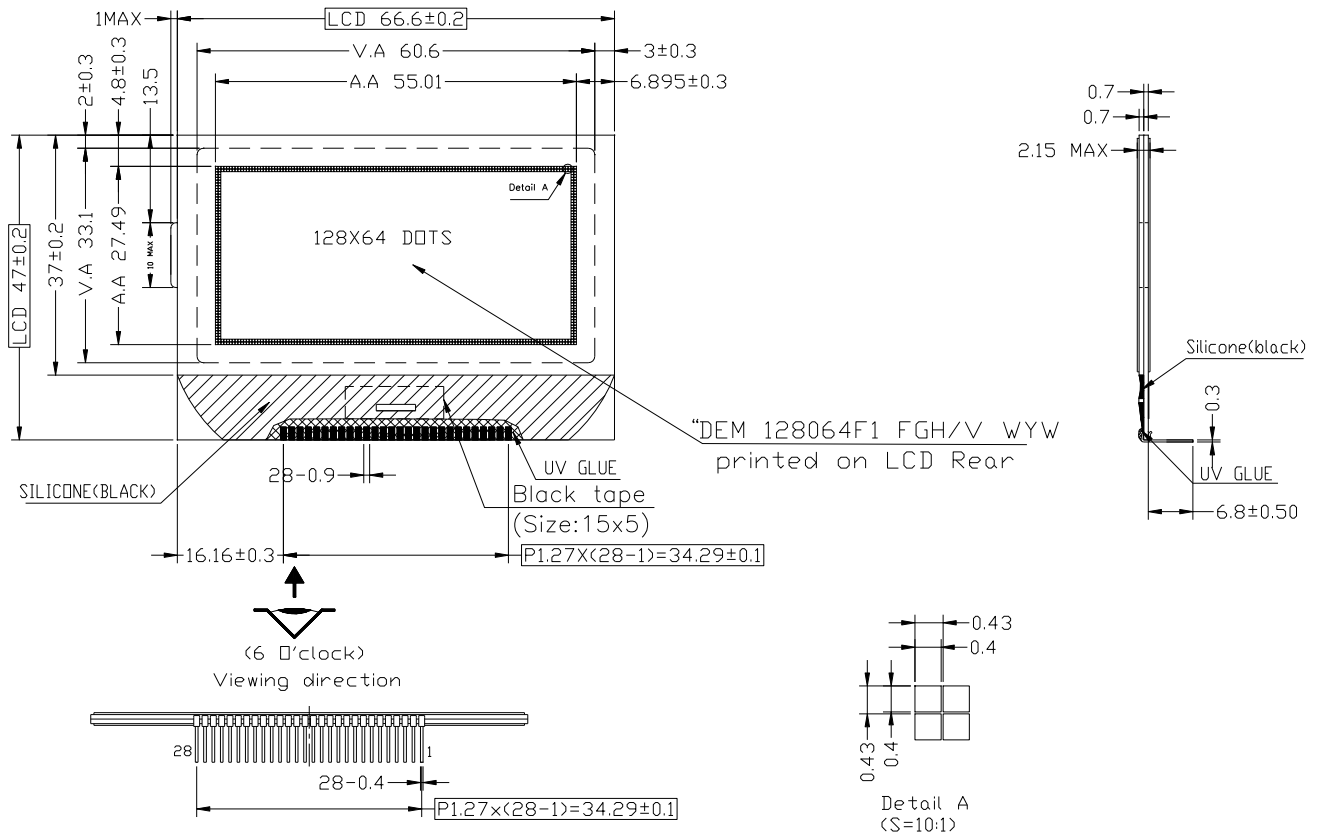| Module	LCD Type	Remarks
DEM 128064F1 FGH	FSTN Reflective positive Mode	

- Viewing Direction   : 6 O'clock
- Driving Scheme   : 1/65 Duty Cycle, 1/9 Bias
- Power Supply Voltage(Typ.)   : 3.0 V
- LCD Operation Voltage   : 9.8 V
- Display Contents   :128x64 Dots
- Interface   : Parallel & Serial
- Driver IC   : IST3004-TX
- RoHS Compliant

2. MECHANICAL SPECIFICATIONS

- Module Size   : 66.60 x 47.00 x 2.15mm
- Viewing Area   : 60.60 x 33.10 mm
- Active Area   : 55.01 x 27.49mm
- Dot pitch   : 0.43 x 0.43mm
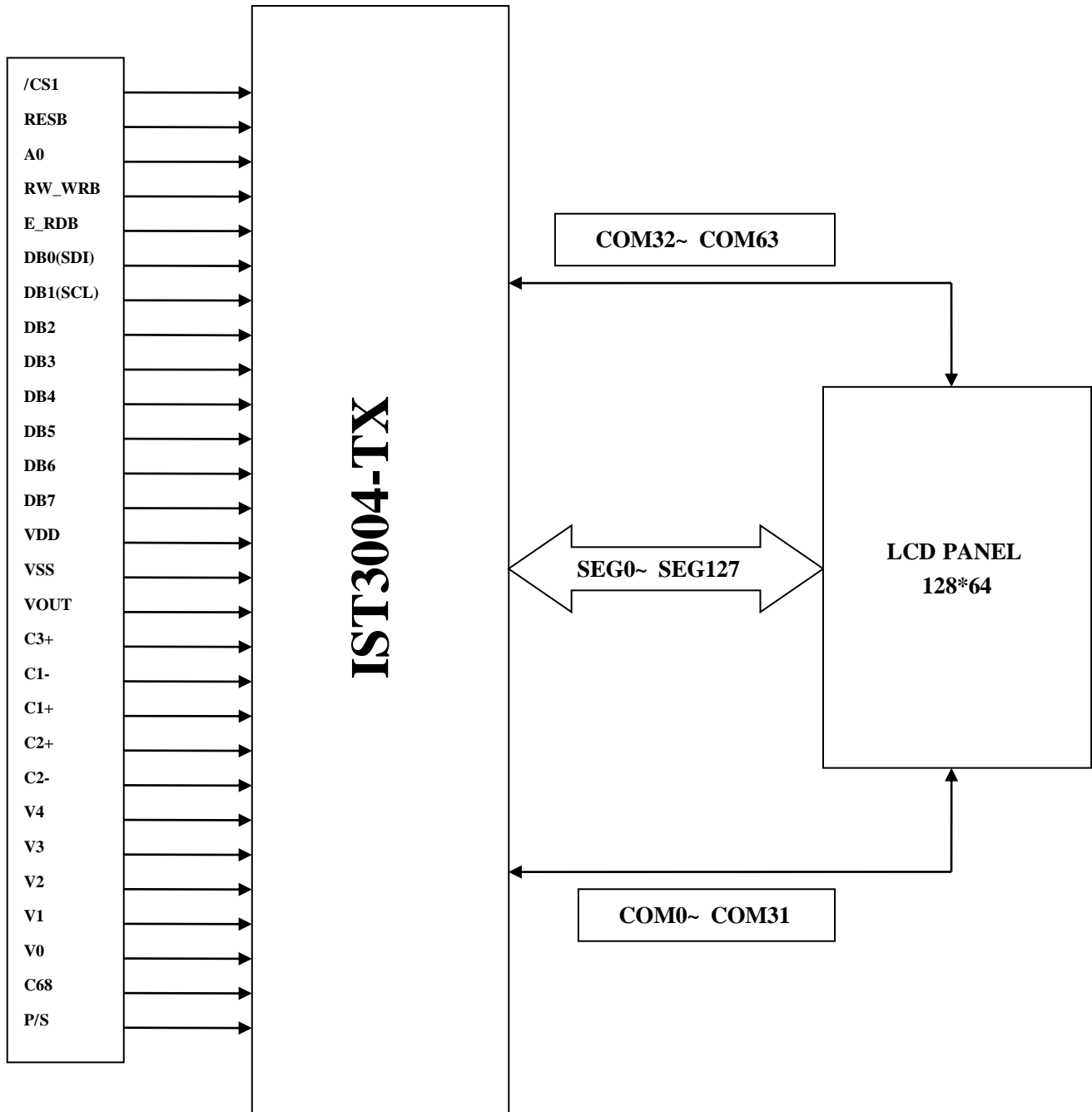- Dot Size   : 0.40 x 0.40 mm
- Dot Gap   :0.03mm

3. EXTERNAL DIMENSIONS

Remarks:
1.Unmarked tolerance is ±0.30;
2.All material comply with RoHs.

4. BLOCK DIAGRAM

Signal	
/CS1	
RESB	
A0	
RW_WRB	
E_RDB	
DB0(SDI)	
DB1(SCL)	
DB2	
DB3	
DB4	
DB5	
DB6	
DB7	
VDD	
VSS	
VOUT	
C3+	
C1-	
C1+	
C2+	
C2-	
V4	
V3	
V2	
V1	
V0	
C68	
P/S	

IST3004-TX

COM32~ COM63

SEG0~ SEG127

LCD PANEL
128*64

COM0~ COM31

5. PIN DESCRIPTION

Pin No.	Name	I/O	Description
1	CS1B	I	Chip select input pins Data / instruction I/O is enabled only when CS1B is "L" and CS2 is "H". when chip select is non-active, DB0 to DB7 may be high impedance
2	RESB	I	Hardware Reset input pin When RESB is "L", initialization is executed.
3	A0	I	Register select input pin - A0 = "H" : DB0 to DB7 are display data - A0 = "L" : DB0 to DB7 are control data
4	RW_WRB	I	Read / Write execution control pin <table><tr><td>C86</td><td>MPU Type</td><td>RW_WRB</td><td>Description</td></tr><tr><td>H</td><td>6800-series</td><td>WR</td><td>Read / Write control input pin - RW = "H" : read - RW = "L" : write</td></tr><tr><td>L</td><td>8080-series</td><td>/WRB</td><td>Write enable clock input pin The data on DB0 to DB7 are latched at the rising edge of the /WRB signal.</td></tr></table>
5	E_RDB	I	Read / Write execution control pin <table><tr><td>C86</td><td>MPU Type</td><td>E_RDB</td><td>Description</td></tr><tr><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin - RW = "H" : When E is "H", DB0 to DB7 are in an output status. - RW = "L" : The data on DB0 to DB7 are latched at the falling edge the E signal.</td></tr><tr><td>L</td><td>8080-series</td><td>/RDB</td><td>Read enable clock input pin When / RDB is "L", DB0 to DB7 are in an output status.</td></tr></table>
6~13	DB0~DB7	I/O	8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = "L"); - DB0 to DB5 : high impedance - DB6 : serial input clock (SCL) - DB7 : serial input data (SDI) When chip select is not active, DB0 to DB7 may be high impedance.
14	VDD	Power Supply	Power supply for logic.
15	VSS	Power Supply	Ground.
16	Vout	I/O	DC/DC voltage converter
17	C3+	O	
18	C1-	O	
19	C1+	O	
20	C2+	O	
21	C2-	O	
22	V4	I/O	LCD driver supply voltages The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application. Voltages should have the following relationship; $V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS$ When the internal power circuit is active, these voltages are generated as following as following table according to the state of LCD bias. <table><tr><td>LCD bias</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr><tr><td>1/9bias</td><td>(8/9) xV0</td><td>(7/9) xV0</td><td>(2/9) xV0</td><td>(1/9) xV0</td></tr></table>
23	V3		
24	V2		
25	V1		
26	V0		
27	C68	I	Microprocessor Interface Select input pin in parallel mode - C68 = "H" : 6800-series MPU interface - C68 = "L" : 8080-series MPU interface
28	P/S	I	Parallel / serial data input select input <table><tr><td>PS</td><td>Interface Mode</td><td>Chip Select</td><td>Data / instruction</td><td>Data</td><td>Read / Write</td><td>Serial clock</td></tr><tr><td>"H"</td><td>Parallel</td><td>CS1B</td><td>A0</td><td>DB0 to DB7</td><td>E_RDB RW_WRB</td><td>--</td></tr><tr><td>"L"</td><td>Serial</td><td>CS1B</td><td>A0</td><td>SDI (DB7)</td><td>Write only</td><td>SCL (DB6)</td></tr></table> < NOTE> In serial mode, it is impossible to read data from the on-chip RAM. And DB0 to DB5 and E_RDB and RW_WRB must be fixed to either "H" or "L".

6. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Unit
Power Supply Voltage	VDD	-0.3 ~ 7.0	V
Power supply voltage (VDD standard)	V0, VOUT	-0.3 ~ 15.0	V
Power supply voltage (VDD standard)	V1, V2, V3, V4	-0.3 to V0	V
Operating temperature	TOPR	–20 to +70	°C
Storage temperature	TSTR	–30 to +80	°C

7. ELECTRICAL CHARACTERISTICS

7.1. DC CHARACTERISTICS

Item	Symbol	Condition	STANDARD VALUE			Unit
			Min.	Typ.	Max.	
Operating Voltage	V_{DD}	-	2.7	3.0	3.3	V
LCD driving voltage	V_{LCD}	V0-VSS	9.6	9.8	10	
Consumption current	I_{DD}	Display pattern character	-	0.27	0.41	mA
	I_{DD}	Display pattern checker	-	0.6	0.9	mA

7.2. AC CHARACTERISTICS

Read / Write Characteristics (8080-series MPU)
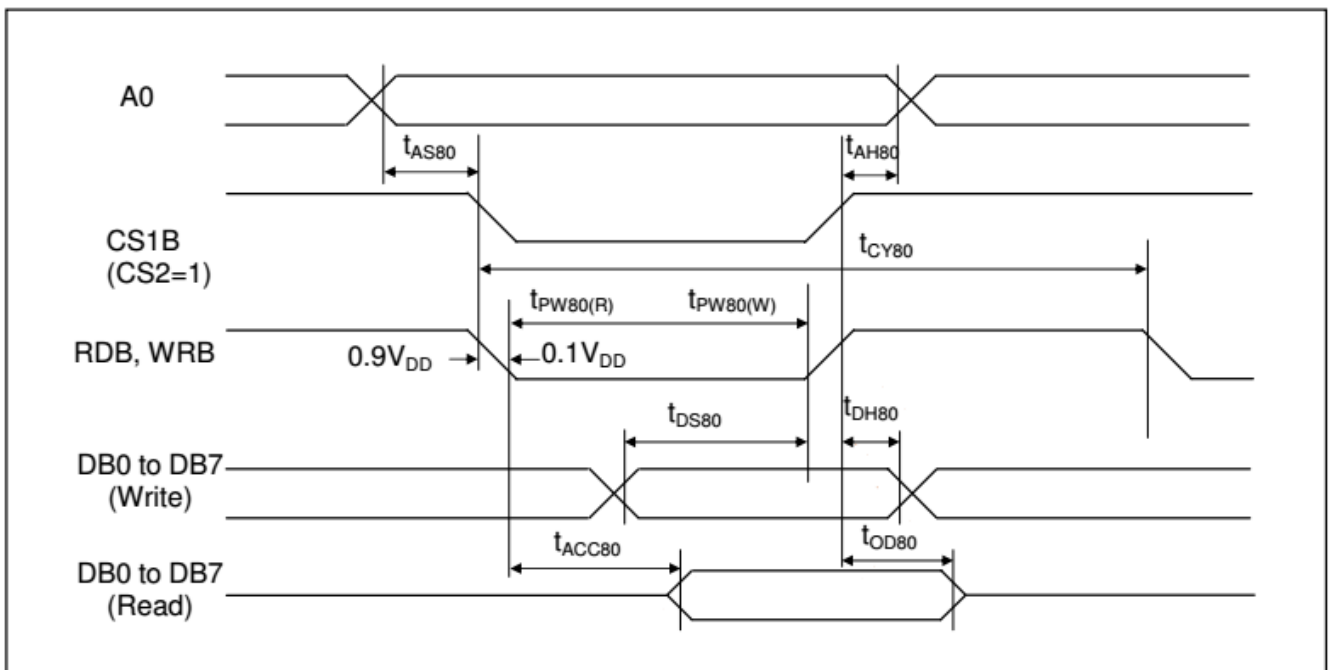
Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	A0	tAS80 tAH80	0 0	-	-	ns	
System cycle time		tCY80	300	-	-	ns	
Pulse width (WRB)	RW_WRB	tPW80(W)	150	-	-	ns	
Pulse width (RDB)	E_RDB	tPW80(R)	150	-	-	ns	
Data setup time Data hold time	DB7 to DB0	tDS80 tDH80	60 0	-	-	ns	
Read access time Output disable time		tACC80 tOD80	140 -	-	- 10	ns	(No load)

Read / Write Characteristics (6800-series Microprocessor)
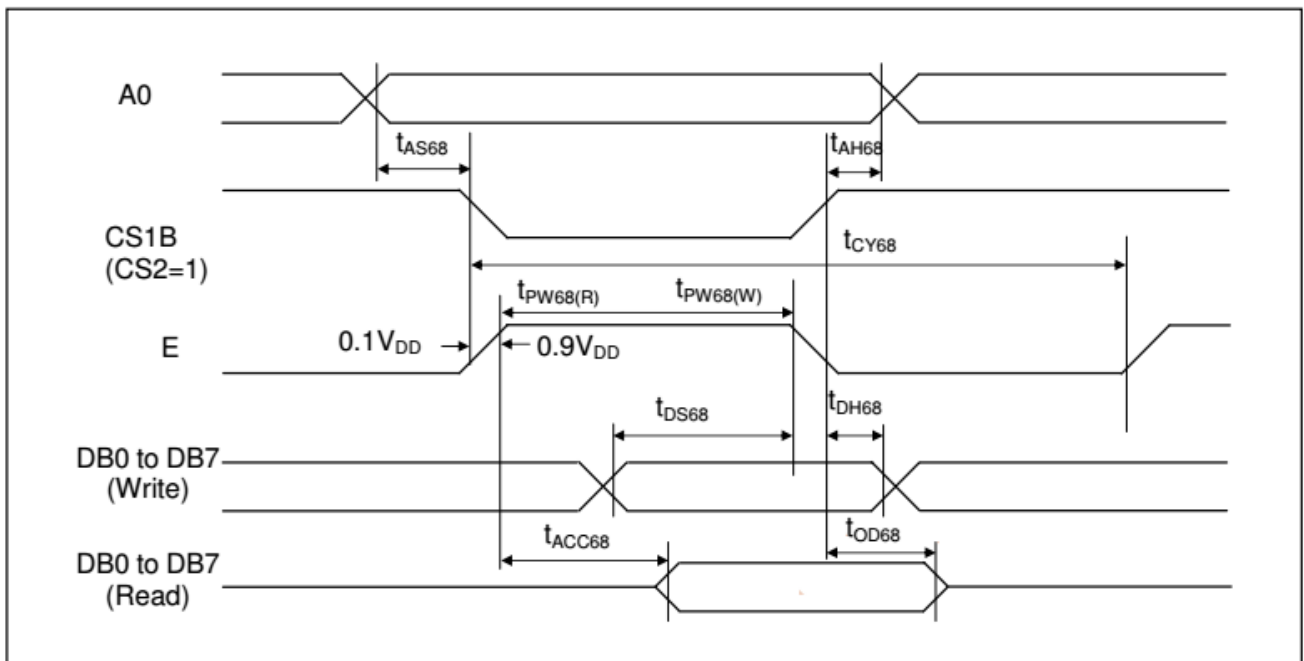
Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	A0	tAH68	0 0	-	-	ns	
System cycle time		tCY68	300	-	-	ns	
Pulse width (E)	RW_WRB	tPW68(W)	150	-	-	ns	
Pulse width (E)	E_RDB	tPW68(R)	150	-	-	ns	
Data setup time Data hold time	DB7 to DB0	tDS68 tDH68	60 0	-	-	ns	
Read access time Output disable time		tACC68 tOD68	140 -	-	- 10	ns	(No load)

Serial Interface Characteristics
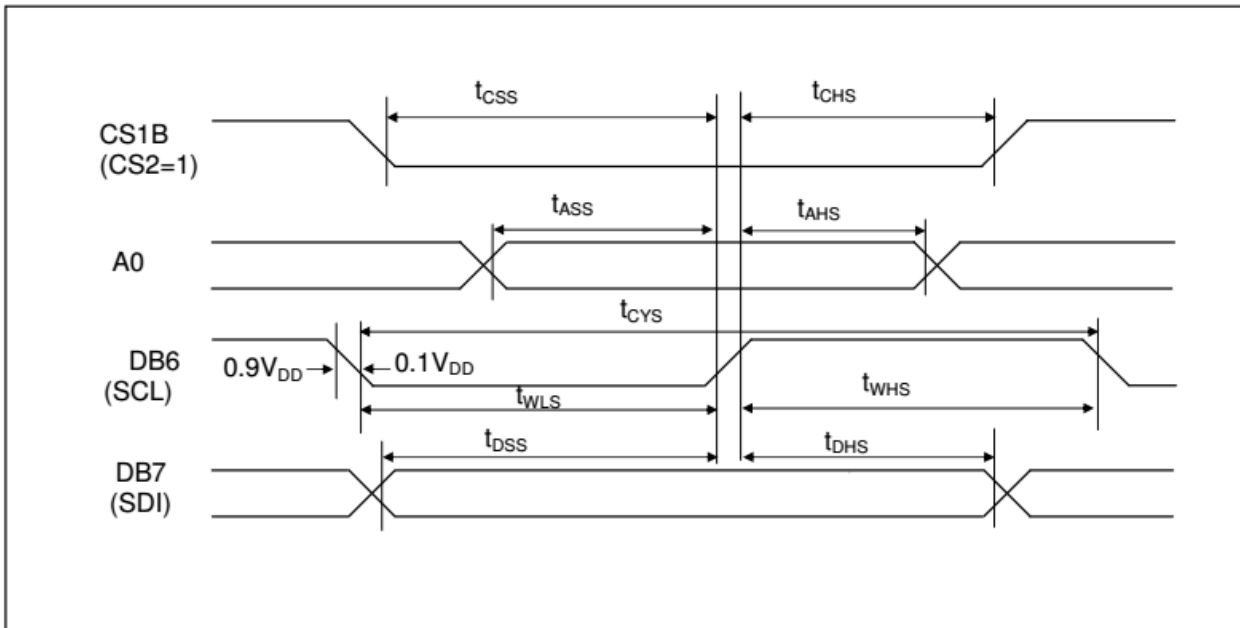
Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle	DB6 (SCL)	tCYS	200	-	-	ns	
SCL high pulse width		tWHS	90	-	-		
SCL low pulse width		tWLS	90	-	-		
Address setup time	A0	tASS	45	-	-	ns	
Address hold time		tAHS	45	-	-		
Data setup time	DB7 (SDI)	tDSS	45	-	-	ns	
Data hold time		tDHS	45	-	-		
CS1B setup time	CS1B	tCSS	90	-	-	ns	
CS1B hold time		tCHS	90	-	-		

Reset Input Timing
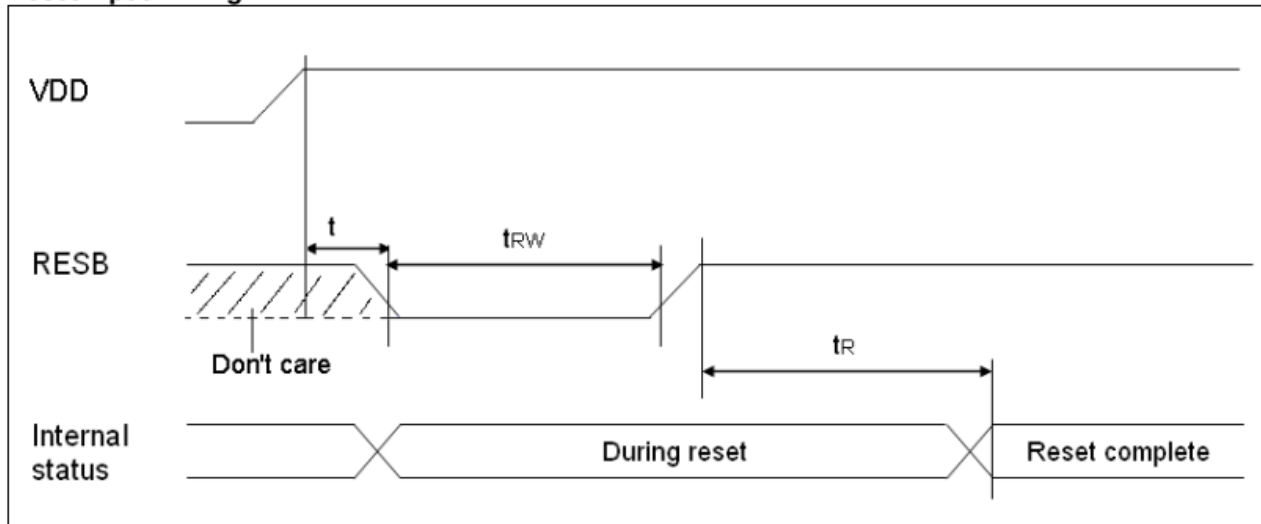
Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	RESB	tRW	2	-	-	us	
Reset time	-	tR	-	-	2	us	
Reset time	RESB	t	0	-	-	us	

8. COMMAND TABLE

INSTRUCTION	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Display ON / OFF	0	0	1	0	1	0	1	1	1	DON	LCD display On/Off control DON = 0 : display OFF DON = 1 : display On
Display starting line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify the line address for the first COM output
page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	Y7	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
Read status	0	1	BUSY	ADC	ON/OFF	RESB	0	0	0	0	Read the internal status
Write display data	1	0	Write data								Write data into Display RAM
Read display data	1	1	Read data								Read data from Display RAM
ADC select	0	0	1	0	1	0	0	0	0	ADC	SEG output direction select ADC = 0 : SEG0 → SEG131 ADC = 1 : SEG131 → SEG0
Reverse display ON / OFF	0	0	1	0	1	0	0	1	1	REV	Normal / Reverse display select REV = 0 : Reverse display off REV = 1 : Reverse display on
Entire display ON / OFF	0	0	1	0	1	0	0	1	0	EON	Entire display On/Off control EON = 0 : Entire display off EON = 1 : Entire display on
LCD bias select	0	0	1	0	1	0	0	0	1	BS	Select LCD bias
Set Read-modify-write (RMW)	0	0	1	1	1	0	0	0	0	0	Set Read-modify-write mode
Clear RMW	0	0	1	1	1	0	1	1	1	0	Clear Read-modify-write mode
S/W Reset	0	0	1	1	1	0	0	0	1	0	S/W Reset
SHL select	0	0	1	1	0	0	SHL	×	×	×	COM output direction select SHL = 0 : COM0 → COM63 SHL = 1 : COM63 → COM0
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Regulator resistor select	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set reference voltage mode	0	0	1	0	0	0	0	0	0	1	Set reference voltage mode (double byte command)
Set reference voltage register	0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0	Set reference voltage register
Set static indicator mode	0	0	1	0	1	0	1	1	0	SM	Set static indicator mode (double byte command)
Set static indicator register	0	0	×	×	×	×	×	×	S1	S0	Set static indicator register
Power save	·	·	·	·	·	·	·	·	·	·	Compound Instruction of display OFF and entire display ON
NOP	0	0	1	1	1	0	0	0	1	1	No operation (dummy command)
Set Booster Ratio select mode	0	0	1	1	1	1	1	0	0	0	Set Booster ration select mode (double byte command)
Set Booster Ratio register	0	0	×	×	×	×	×	×	BT1	BT0	Set Booster ration BT[1:0] = 00 : x2, x3, x4 BT[1:0] = 01 : x5 BT[1:0] = 11 : x6 BT[1:0] = 10 : (don't use)
Test Instruction	0	0	1	0	0	0	1	0	0	0	Test command (don't use)

9. MODULE ACCEPTS QUALITY LEVEL (AQL)

9.1. AQL standard value: Critical defect =0.1, Major defect=0.65; Minor defect =2.5.
9.2. Inspection Standard: MIL-STD-105E Table Normal Inspection Single Sampling Level Ⅱ.

10. RELIABILITY TEST

Operating life time: 50,000 hours
   (at room temperature without direct irradiation of sunlight)
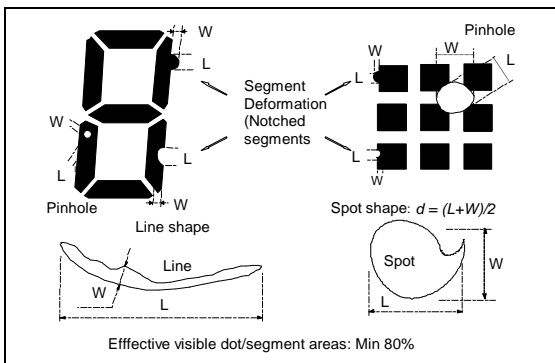Reliability characteristics shall meet following requirements.

Tests Item	Condition
High temperature storage	+80℃ x 96HR
Low temperature storage	-30℃ x 96HR
High temperature operation	+70℃ x 96HR
Low temperature operation	-20℃ x 96HR
High temperature, High humidity	+60℃ x 90%RH x 96HR
Thermal shock	-20℃ x 30min → 25℃ x 10s → +60℃ x 30 min x 5 cycles
Vibration test	Frequency x Swing x Time 40Hz x 4mm x 4hrs
Drop test	Height x no. of drop 1.0m x 6 drops

11. QUALITY DESCRIPTION

DEFECT SPECIFICATION:

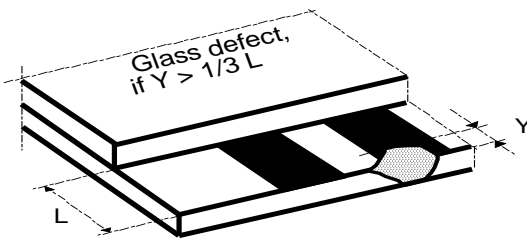Specific type-related items are covered in this sheet.

a: Table for Cosmetic defects

         (Note: nc = not counted).

         Sizes and number of defects

         (Max. Qty)

Defect Type	Max. defect size [μm] d or L W	Max. Quantity.
Black or White Spots	d ≤ 150	nc
	150< d ≤ 300	5
Black or White Lines	W ≤ 10	nc
	L ≤ 5000 W ≤ 30	3
	L ≤ 2000 W ≤ 50	2
Pinhole	d ≤ 150 150< d ≤ 300	nc 1/segment
(Total defects)		(5)
Segment Deformation	W ≤ 100	nc
Bubble (e.g. under pola)	d ≤ 150	nc
	200< d ≤ 400	3
	400< d ≤ 600	1

Effective visible dot/segment areas: Min 80%

Examples/ Shapes

b: Glass defects

b1:Glass defects at contact ledge

b2:Glass chipping in other areas shall not be in conflict

with the product's function.

12. LCD MODULES HANDLING PRECAUTIONS

■   The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

■   If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.

■   Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

■   The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.

■   To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
    -Be sure to ground the body when handling the LCD module.
    -Tools required for assembly, such as soldering irons, must be properly grounded.
    -To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
    -The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

■   Storage precautions
    When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging (or in bags designed to prevent static electricity charging) under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below -20°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

13. OTHERS

■   Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.

■   If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.

■   To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules:
    - Exposed area of the printed circuit board
    - Terminal electrode sections