

**DISPLAY Elektronik GmbH**

**DATA SHEET**

**LCD MODULE**

**DEM 128064Q FGH**

*Product Specification*

*Version: 5*

**08.02.2018**

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# GENERAL SPECIFICATION

MODULE NO. :

# DEM 128064Q FGH

CUSTOMER P/N:

VERSION NO.	CHANGE DESCRIPTION	DATE
0	Original Version	22.01.2018
1	Correct Segment Layout Correct Pin18 and Pin 21 Symbol	24.01.2018
2	Correct the FPC to the LCD bottom side	29.01.2018
3	Change the IC to UC1601x Correct the AC Characteristics Correct the LCD Layout Correct the BL drawing	05.02.2018
4	Correct "LCD ARTWORK" in the header line	06.02.2018
5	Correct FPC pin No. in the module drawing	08.02.2018

PREPARED BY: PS

DATE: 08.02.2018

APPROVED BY: MH

DATE: 08.02.2018

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**1. FUNCTIONS & FEATURES**

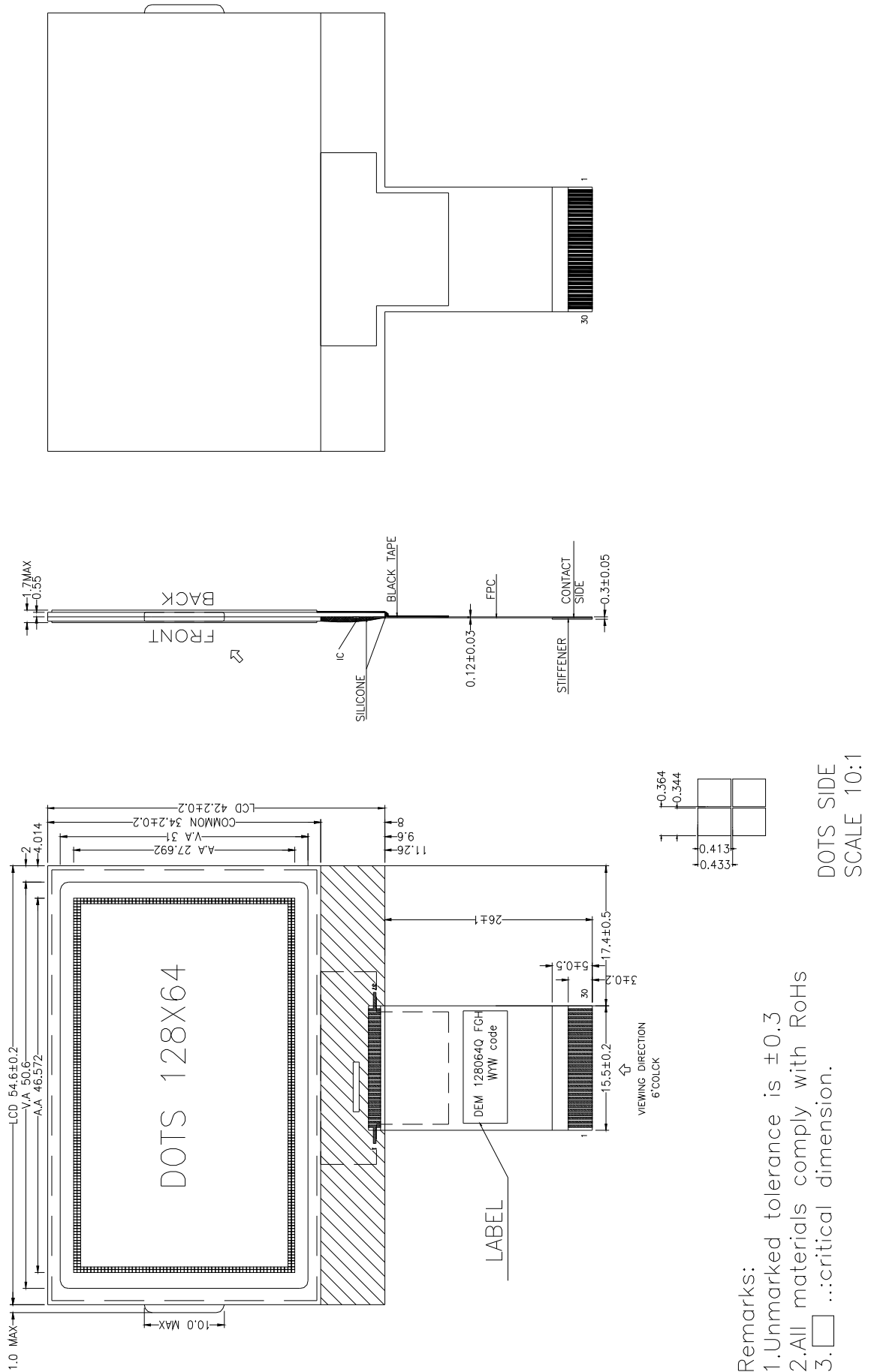
MODULE NAME	LCD TYPE
DEM 128064Q FGH	FSTN Reflective Positive

- Viewing Direction : 6 O'clock
- Driving Scheme : 1/65 Duty, 1/9 Bias
- Power Supply Voltage : 3 Volt (typ.)
- V<sub>LCD</sub> : 10.2 Volt (typ.)
- Display Contents : 128 x 64 Dots
- Driver IC : UC1601x (Ultrachip)

**2. MECHANICAL SPECIFICATIONS**

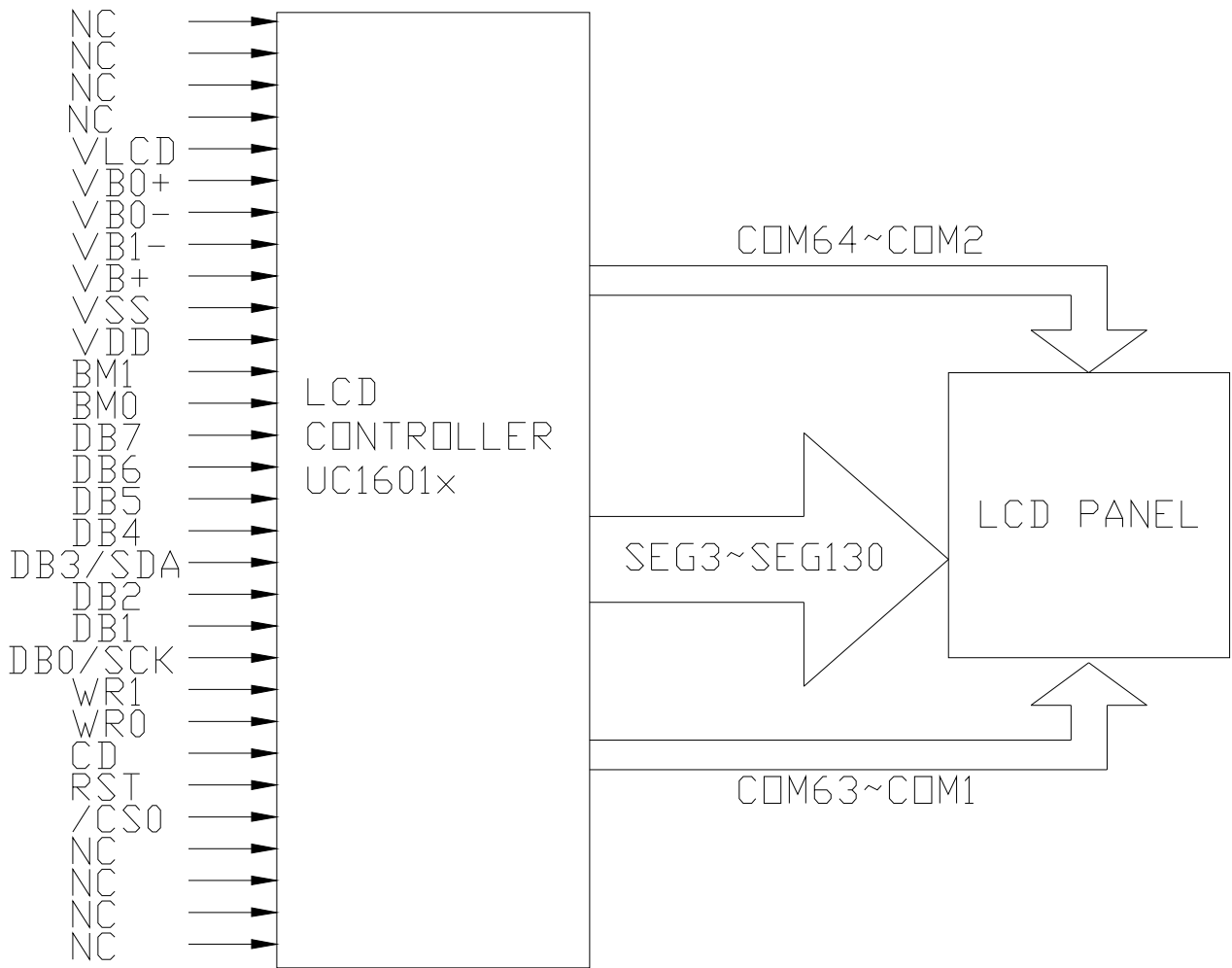
- Module Size : 54.60 x 42.20 x 1.70 mm
- Viewing Area : 50.60 x 31.00 mm
- Active Area : 46.572 x 27.692 mm

3. EXTERNAL DIMENSIONS



- Remarks:
1. Unmarked tolerance is ±0.3
  2. All materials comply with RoHs
  3. □ ∴ critical dimension.

4. BLOCK DIAGRAM



5. PIN ASSIGNMENT

Pin No	Symbol	Description																																														
1~4	NC	No Connection																																														
5	VLCD	Main LCD Power Supply																																														
6	VB0+	LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally Connect capacitors of C <sub>bx</sub> value between V <sub>bx+</sub> and V <sub>bx-</sub>																																														
7	VB0-																																															
8	VB1-																																															
9	VB1+																																															
10	VSS	Power Ground																																														
11	VDD	Power supply terminal VCC																																														
12	BM1	Bus mode: “HL”:8080 “HH”:6800																																														
13	BM0	BM[1:0] “LH”:S9 “LL”:S8																																														
14	DB7	Bi-directional bus for both serial and parallel host interfaces in serial modes connect DB0 to SCK,DB3 to SDA																																														
15	DB6																																															
16	DB5																																															
17	DB4																																															
18	DB3/SDA																																															
19	DB2																																															
20	DB1																																															
21	DB0/SCK		<table border="1"> <thead> <tr> <th></th> <th>BM=1X (8-bit)</th> <th>BM=00 (S8)</th> <th>BM=01 (S9)</th> <th>BM=01 (I<sup>2</sup>C)</th> </tr> </thead> <tbody> <tr> <td>D0</td> <td>D0</td> <td>SCK</td> <td>SCK</td> <td>SCK</td> </tr> <tr> <td>D1</td> <td>D1</td> <td>--</td> <td>--</td> <td>--</td> </tr> <tr> <td>D2</td> <td>D2</td> <td>--</td> <td>--</td> <td>--</td> </tr> <tr> <td>D3</td> <td>D3</td> <td>SDA</td> <td>SDA</td> <td>SDA</td> </tr> <tr> <td>D4</td> <td>D4</td> <td>--</td> <td>--</td> <td>--</td> </tr> <tr> <td>D5</td> <td>D5</td> <td>--</td> <td>--</td> <td>--</td> </tr> <tr> <td>D6</td> <td>D6</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>D7</td> <td>D7</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>		BM=1X (8-bit)	BM=00 (S8)	BM=01 (S9)	BM=01 (I <sup>2</sup> C)	D0	D0	SCK	SCK	SCK	D1	D1	--	--	--	D2	D2	--	--	--	D3	D3	SDA	SDA	SDA	D4	D4	--	--	--	D5	D5	--	--	--	D6	D6	0	0	1	D7	D7	1	1	1
				BM=1X (8-bit)	BM=00 (S8)	BM=01 (S9)	BM=01 (I <sup>2</sup> C)																																									
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D5	D5	--	--	--																																												
D6	D6	0	0	1																																												
D7	D7	1	1	1																																												
22	WR1	WR[1:0]controls the read/write operation of the host interface See Host Interface section for details																																														
23	WR0																																															
24	CD	Select Control data or Display data for read/write operation in S9 CD pin is not used Connect CD to Vss when not used “L”:Control data “H”:Display data																																														
25	RST	Reset																																														
26	/CS0	When /CS=L, then the chip select becomes active																																														
27~30	NC	No Connection																																														

**6. ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Digital Power Supply Voltage	V <sub>DD</sub>	-0.3	+4.0	V
Analog Power Supply Voltage	V <sub>DD2</sub>	-0.3	+4.0	V
Analog Circuit Supply Voltage	V <sub>DD3</sub>	-0.3	+4.0	V
Voltage Difference between VDD and VDD2/3	VDD2/3-VDD	-----	1.2	V
LCD Generated Voltage	V <sub>LCD</sub>	0.8	11.5	V
Any Input/Output	V <sub>IN</sub> /V <sub>OUT</sub>	-0.4	V <sub>DD</sub> +0.3	V
Operating Temperature	T <sub>opr</sub>	-20	70	□
Storage Temperature	T <sub>STR</sub>	-30	80	□

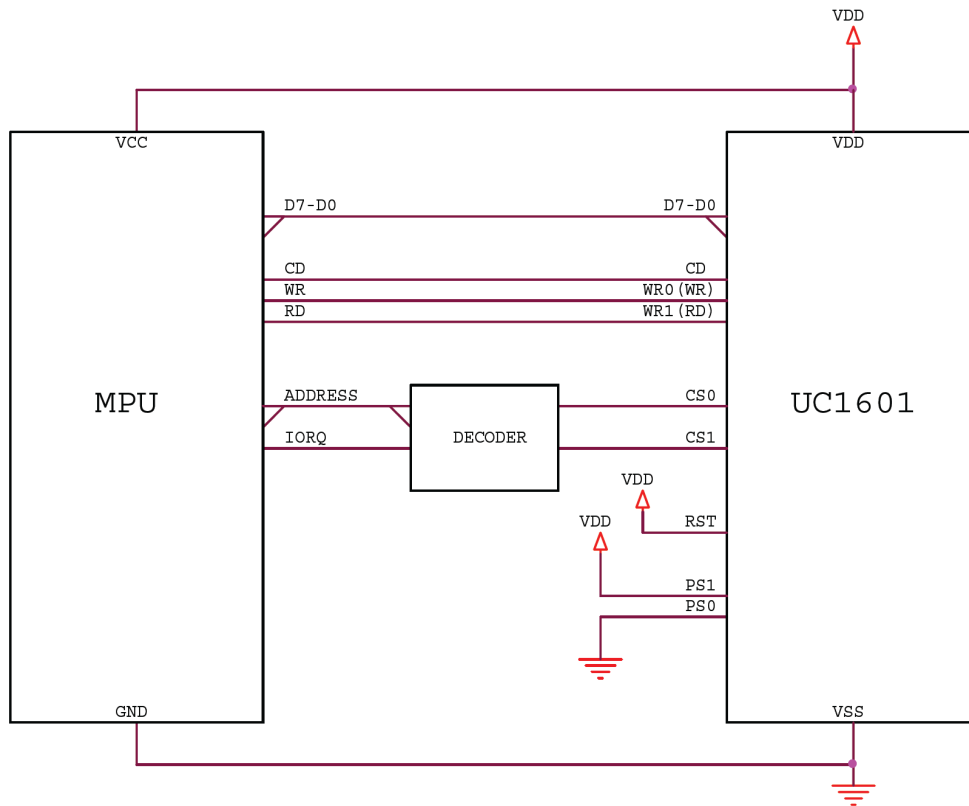
**7. DC CHARACTERISTICS**

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply for LCM	VDD	---	2.7	3	3.3	V
LCD Module Driving Voltage	VLCD	VDD2/3 ≥ 2.4V, +25°C	9.7	10.2	10.7	V
Supply Current for LCM	IDD	---	---	TBD	---	mA

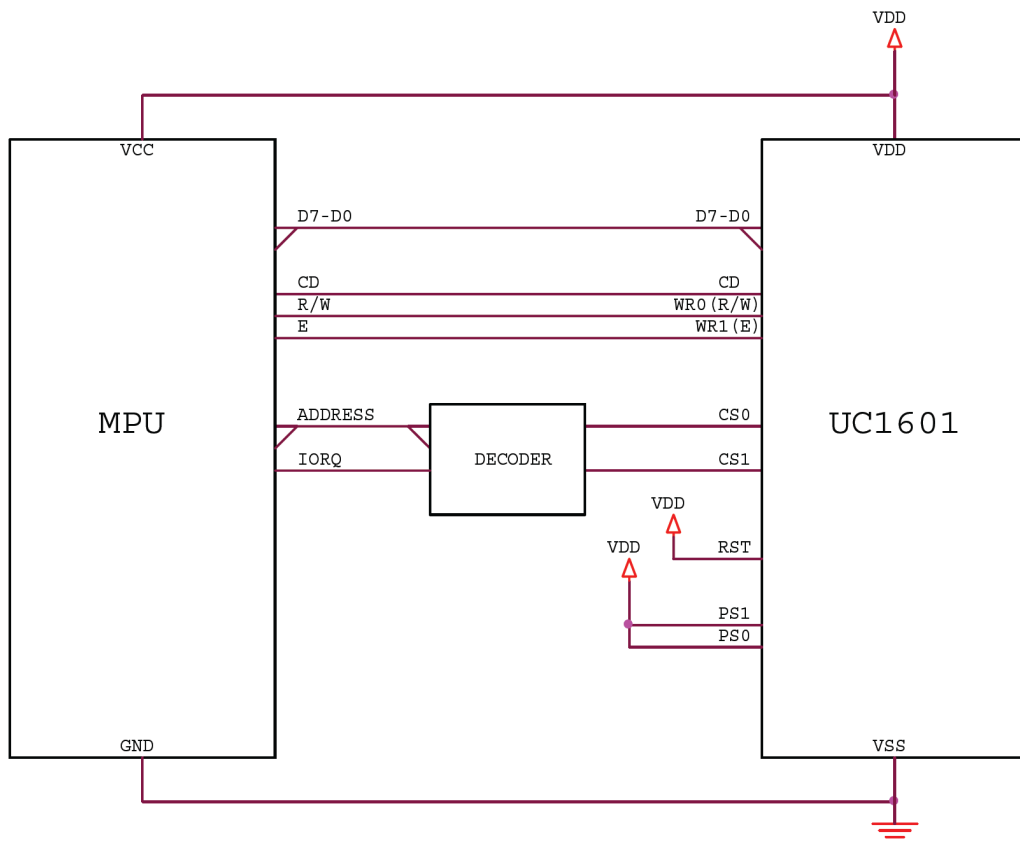


### 8. Voltage Generator Circuit

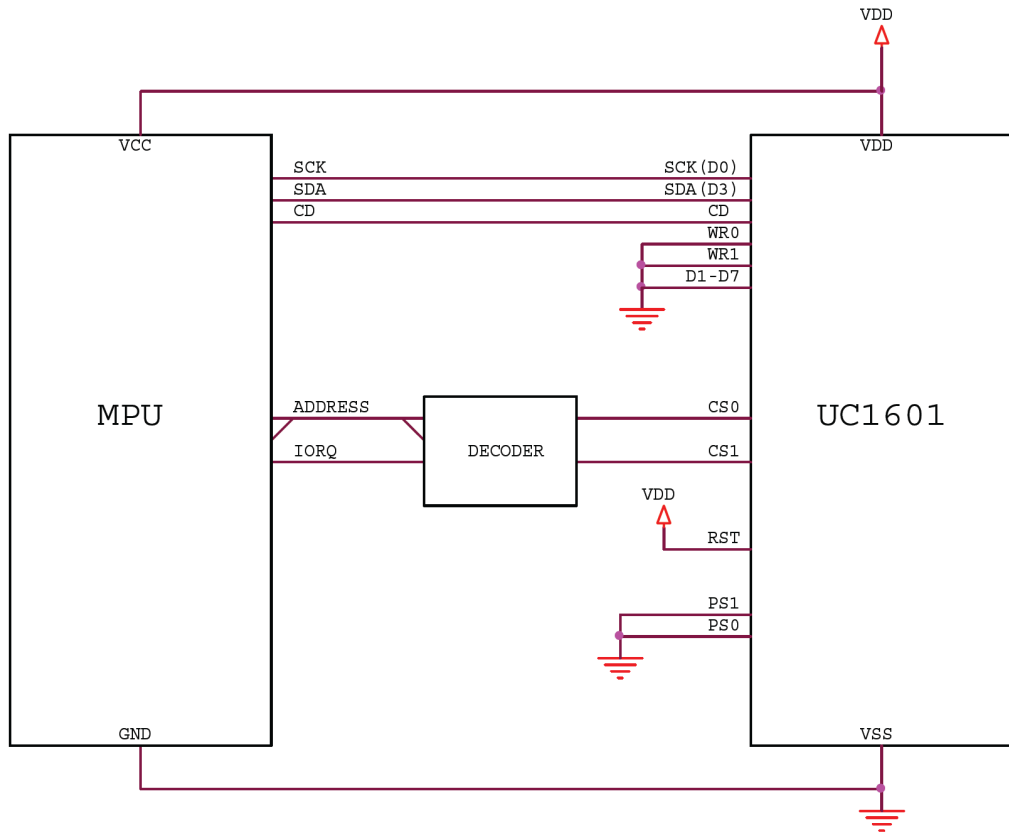
#### 8-1 8080/8bit Parallel Mode Reference Circuit



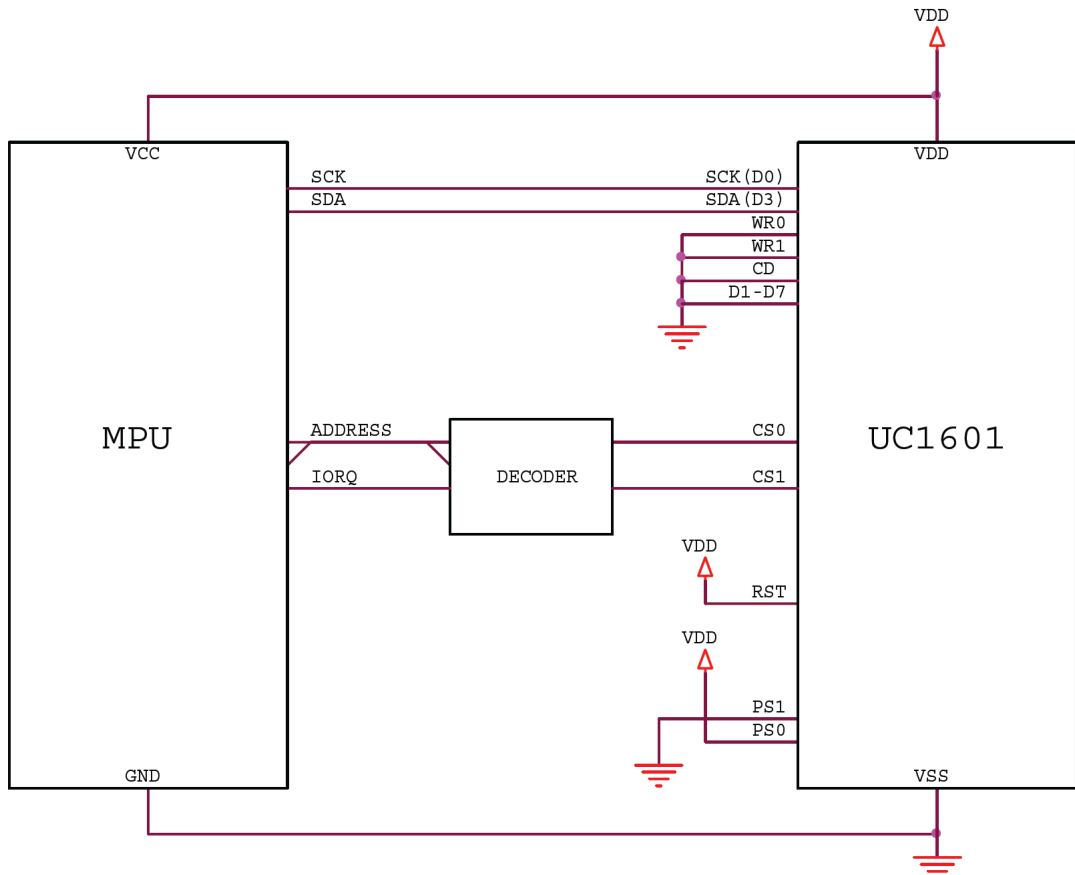
#### 8-2 6800/8bit Parallel Mode Reference Circuit

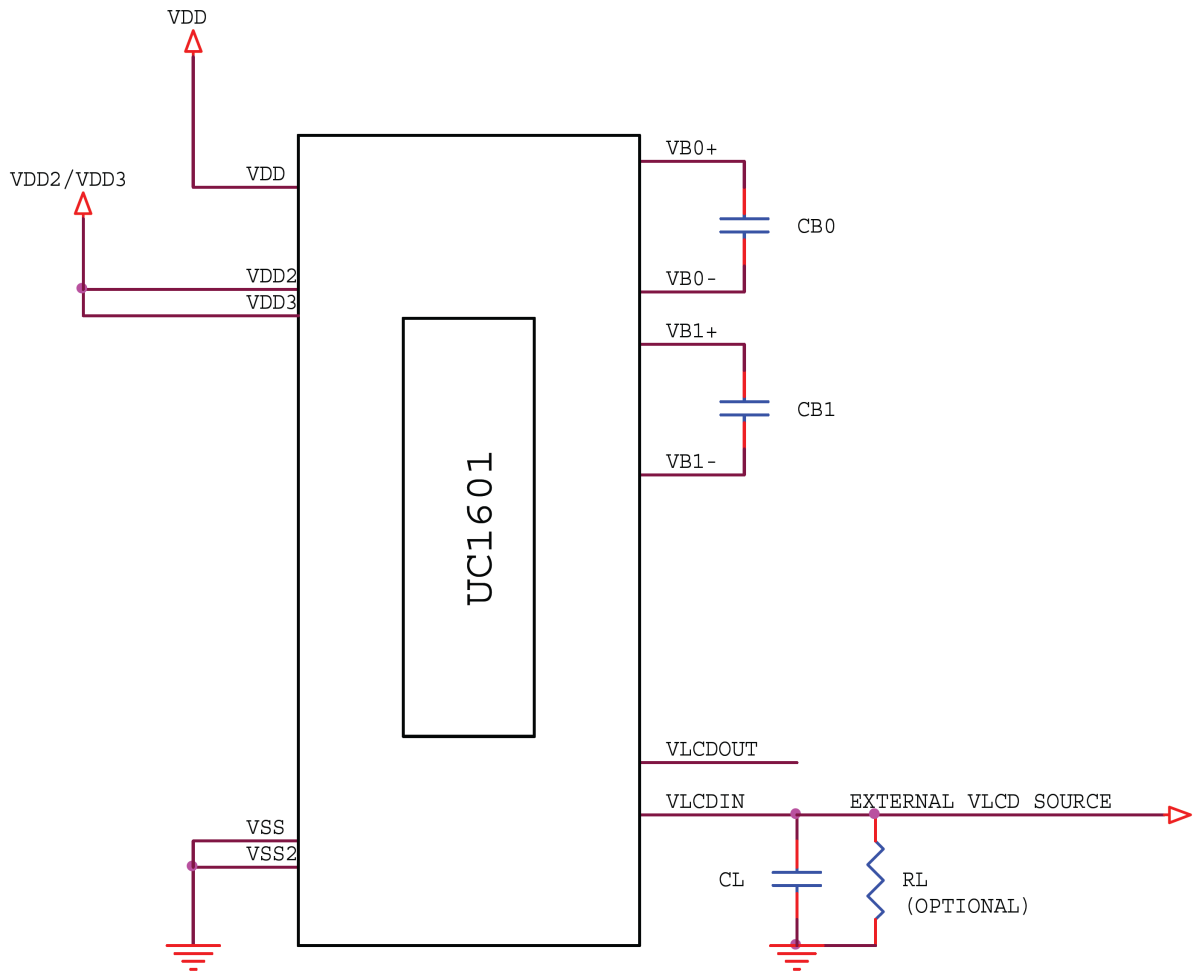


8-3 Serial-8 Serial Mode Reference Circuit



8-4 Serial-9 Serial Mode Reference Circuit





**Note**

Recommended component values:

CB: 100x~200x LCD load capacitance or 1.0uF (2V), whichever is higher.

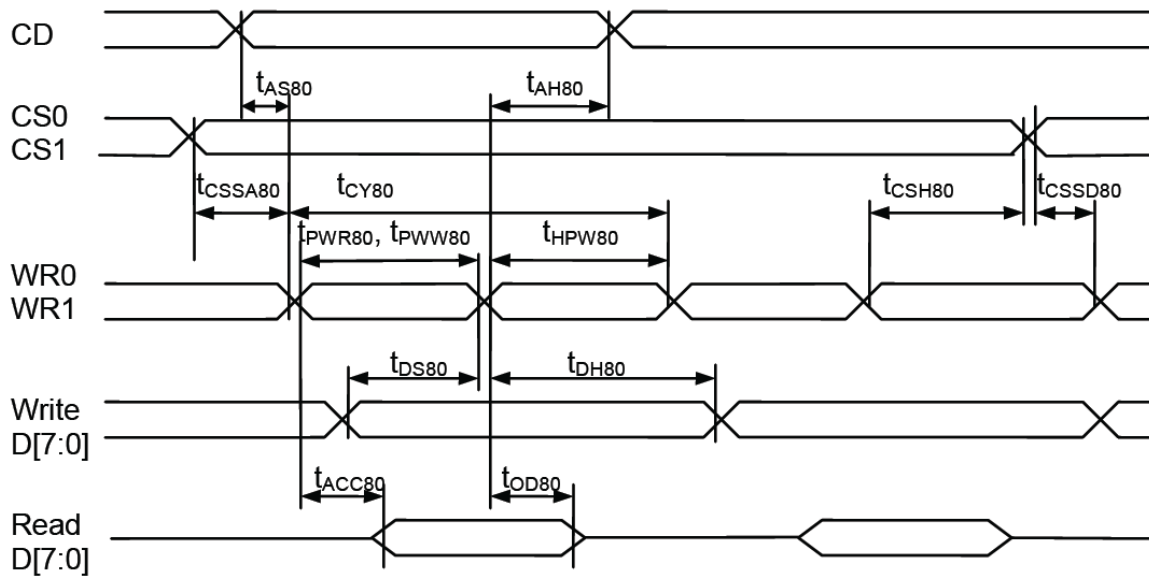
CL: 10nF ~ 30nF (25V) is appropriate for most applications.

RL: 10MΩ. Acts as a draining circuit when the power is abnormally shut down.

The illustrated resistor values are for reference only. Please optimize for specific requirements of each application.

9. AC Characteristics

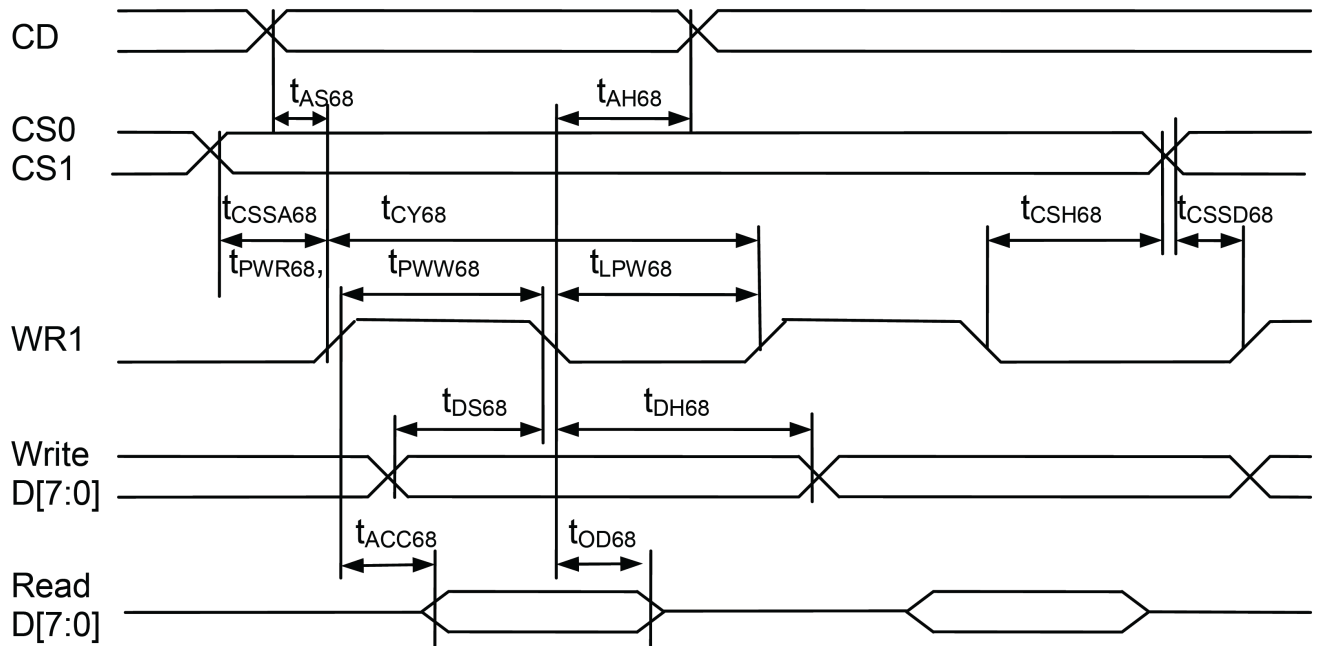
9-1 System Bus Timing for 8080 Series MPU



Parallel Bus Timing Characteristics (for 8080 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(Read / Write)						
$t_{AS80}$ $t_{AH80}$	CD	Address setup time Address hold time		0 40	–	nS
$t_{CSSA80}$ $t_{CSSD80}$ $t_{CSH80}$	CS1/CS0	Chip select setup time		10 10 20	–	nS
$t_{CY80}$	WR1 / WR0	System cycle time		165		nS
$t_{PWR80}$ / $t_{PWW80}$		Pulse width		65 / 65	–	
$t_{HPW80}$		High pulse width		65		
$t_{DS80}$ $t_{DH80}$	D0~D7 (Write)	Data setup time Data hold time		30 20	–	nS
$t_{ACC80}$ $t_{OD80}$	D0~D7 (Read)	Read access time Output disable time	$C_L = 100\text{pF}$	– 10	50 50	nS

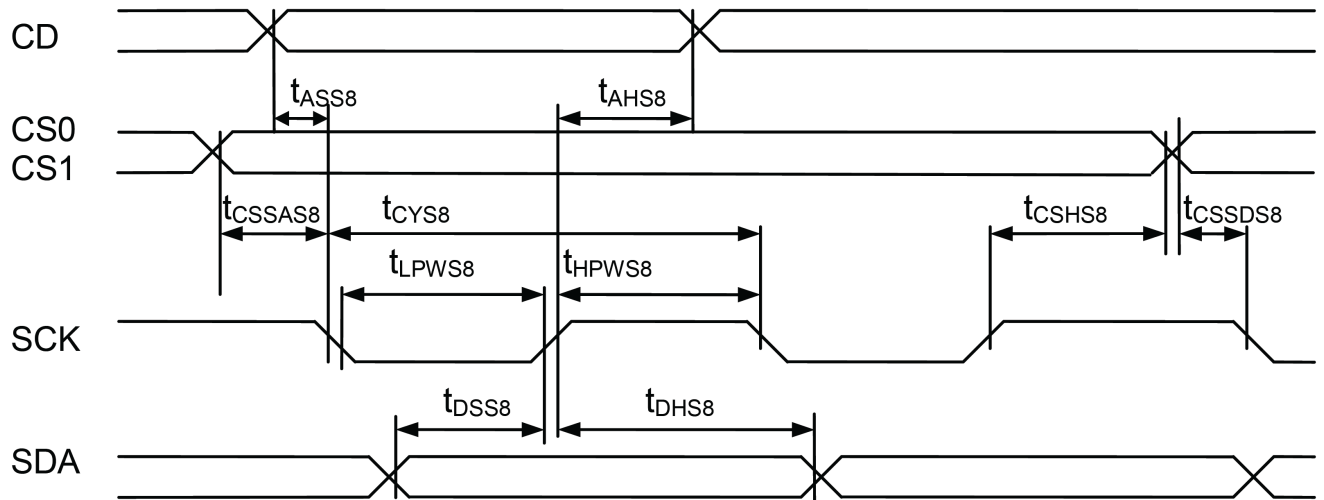
9-2 System Bus Timing for 6800 Series MPU



Parallel Bus Timing Characteristics (for 6800 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(Read / Write)						
$t_{AS68}$	CD	Address setup time		0	-	nS
$t_{AH68}$	CD	Address hold time		40	-	nS
$t_{CSSA68}$	CS1/CS0	Chip select setup time		10	-	nS
$t_{CSSD68}$				10	-	nS
$t_{CSH68}$				20	-	nS
$t_{CY68}$	WR1	System cycle time		160	-	nS
$t_{PWR68} / t_{PWW68}$		Pulse width		65 / 65	-	nS
$t_{LPW68}$		Low pulse width		65	-	nS
$t_{DS68}$	D0~D7 (Write)	Data setup time		30	-	nS
$t_{DH68}$		Data hold time		15	-	nS
$t_{ACC68}$	D0~D7 (Read)	Read access time	$C_L = 100pF$	-	50	nS
$t_{OD68}$		Output disable time		10	50	nS

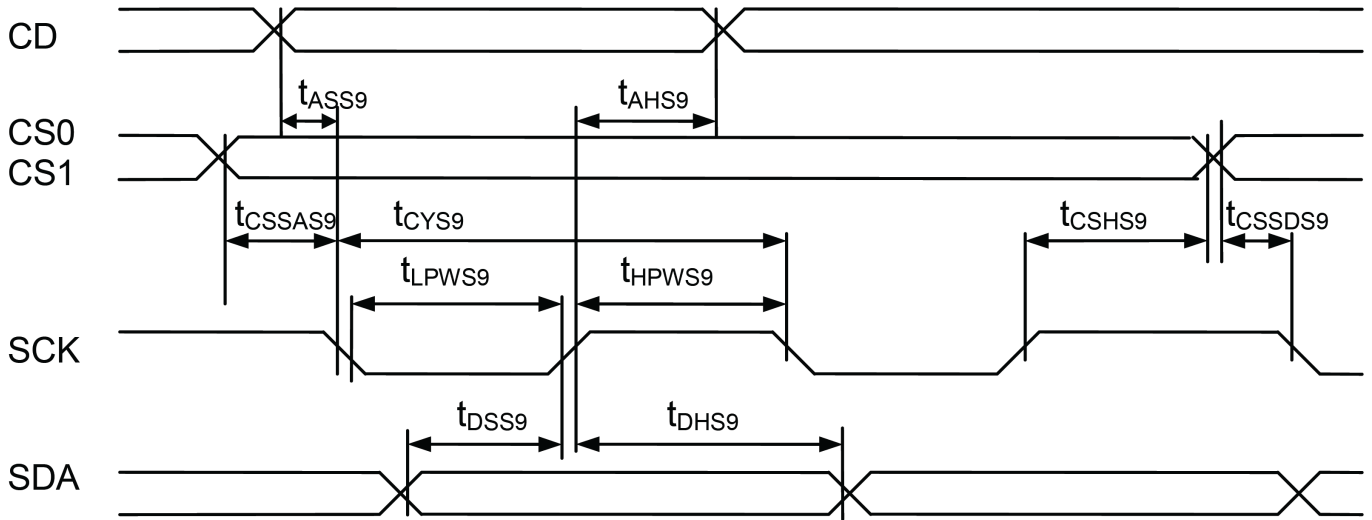
9-3 System Bus Timing for 4-Line Serial Interface



Serial Bus Timing Characteristics (for S8)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(Read / Write)						
$t_{ASS8}$	CD	Address setup time		0	–	nS
$t_{AHS8}$		Address hold time		40	–	nS
$t_{CSSAS8}$	CS1/CS0	Chip select setup time		10		nS
$t_{CSSDS8}$				10	–	
$t_{CSHS8}$				20		
$t_{CYS8}$	SCK	System cycle time		160		nS
$t_{LPWS8}$		Low pulse width		65	–	
$t_{HPWS8}$		High pulse width		65		
$t_{DSS8}$	SDA	Data setup time		30		nS
$t_{DHS8}$		Data hold time		15	–	

9-4 High-Voltage Mixed-Signal IC



Serial Bus Timing Characteristics (for S9)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(Read / Write)						
$t_{ASS9}$	CD	Address setup time		0	–	nS
$t_{AHS9}$		Address hold time		40	–	nS
$t_{CSSAS9}$	CS1/CS0	Chip select setup time		10		nS
$t_{CSSDS9}$				10		
$t_{CSSH9}$				20		
$t_{CYS9}$	SCK	System cycle time		160	–	nS
$t_{LPWS9}$		Low pulse width		65		
$t_{HPWS9}$		High pulse width		65		
$t_{DSS9}$	SDA	Data setup time		30	–	nS
$t_{DHS9}$		Data hold time		15		

10. COMMAND TABLE

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1.	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2.	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3.	Get Status	0	1	-	MX	MY	RS	WA	DE	-		N/A	
4.	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA [3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	#	#	#	#	Set CA [7:4]	0
5.	Set Multiplexing Rate	0	0	0	0	1	0	0	0	#	#	Set MR [1:0]	11b: 65
6.	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b: -0.05%/°C
7.	Set Panel Loading	0	0	0	0	1	0	1	0	0	#	Set PC[0]	0b: ≤ 15nF
8.	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC[2:1]	11b
9.	Set Adv. Program Control (double-byte command)	0	0	0	0	1	1	0	0	0	R	Set APC[R][7:0], R = 0, or 1	N/A
		0	0	#	#	#	#	#	#	#	#		
10.	Set Scroll Line	0	0	0	1	#	#	#	#	#	#	Set SL[5:0]	0
11.	Set Page Address	0	0	1	0	1	1	#	#	#	#	Set PA[3:0]	0
12.	Set V <sub>BIAS</sub> Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	C0H
		0	0	#	#	#	#	#	#	#	#		
13.	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
14.	Set Frame Rate	0	0	1	0	1	0	0	0	0	#	Set LC[3]	0b
15.	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0
16.	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0
17.	Set Display Enable	0	0	1	0	1	0	1	1	1	#	Set DC[2]	0
18.	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	0	Set LC[2:1]	0
19.	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
20.	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
21.	Set Test Control (double-byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
		0	0	#	#	#	#	#	#	#	#		
22.	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 9
23.	Reset Cursor Update Mode	0	0	1	1	1	0	1	1	1	0	AC[3]=0, CA=CR	N/A
24.	Set Cursor Update Mode	0	0	1	1	1	0	1	1	1	1	AC[3]=1, CR=CA	N/A

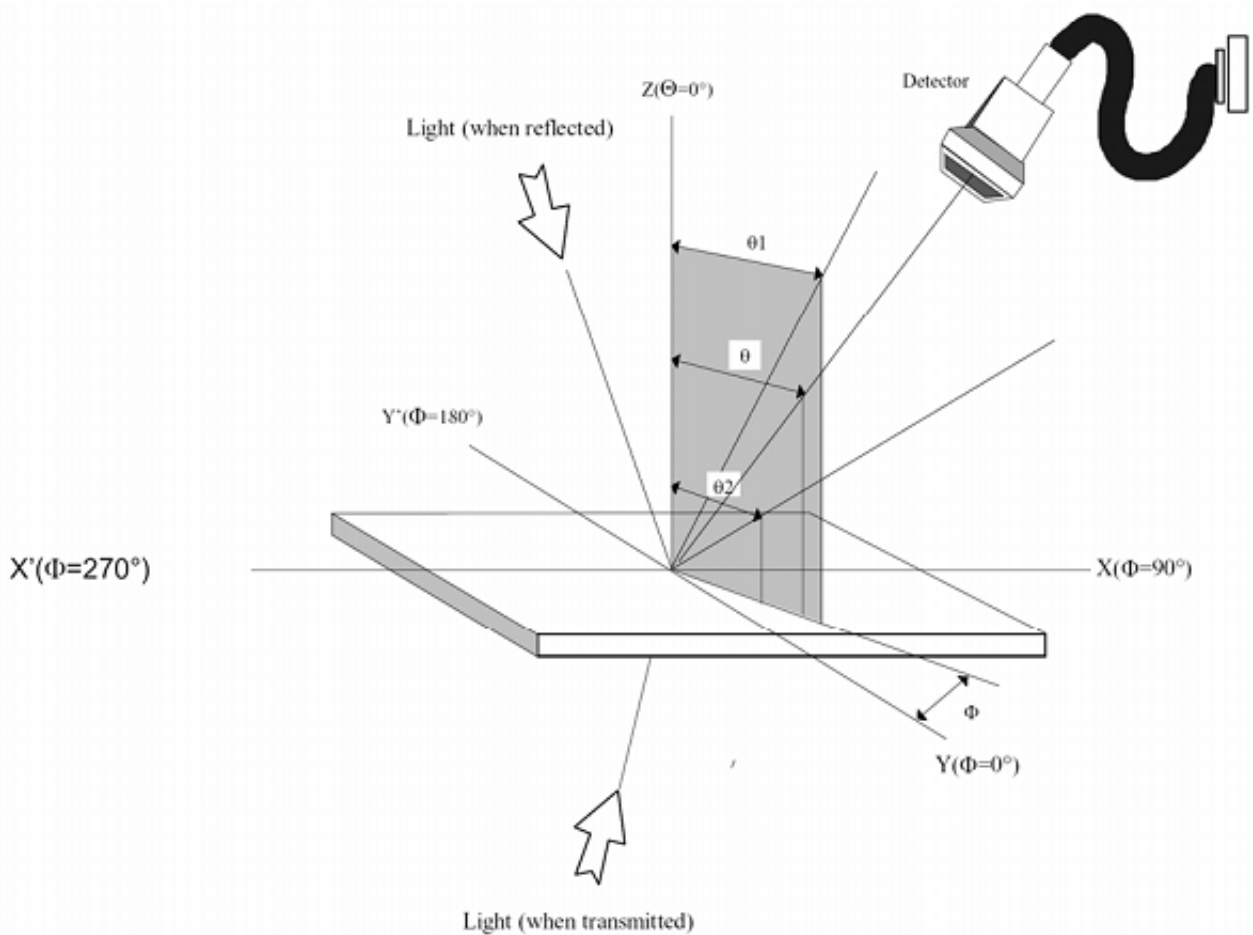
\* Any bit patterns other than what is listed above may result in NOP (No Operation).



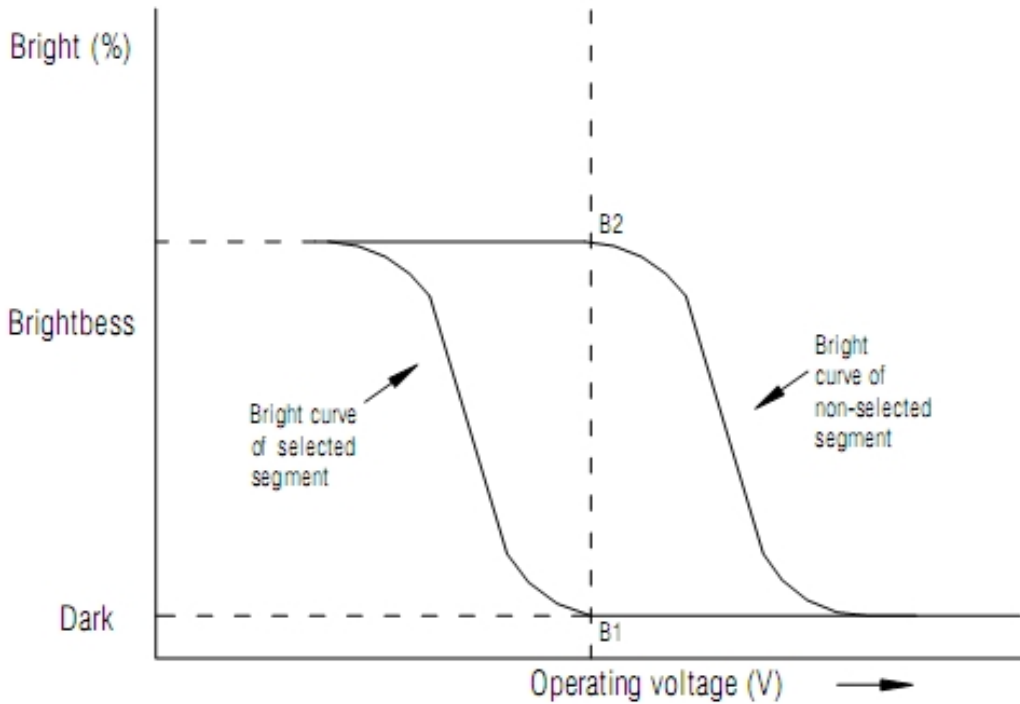
11. LCD ELECTRICAL & OPTICAL CHARACTERISTICS

Item	Symbol	Description	Condition	Temp.	Min.	Typ.	Max.	Unit
Operating Voltage for LCD	$V_{LCD}=VDD-VO$				9.7	10.2	10.7	V
	Vop		Ta=-20°C		11.4	11.9	12.4	
			Ta=+25°C		9.7	10.2	10.7	
			Ta=+70°C		9.2	9.7	10.2	
Contrast	Cr		VDD=3V±3%	+25°C	3.0	---	---	
Viewing Angle	$\theta$	6 o'clock axis ( $\theta=0^\circ$ )	Cr≥2.0 VDD=3V±3%	+25°C	---	30	---	
Response Time	Tr	Rise		+25°C	---	---	198	ms
	Tf	Fall		+25°C	---	---	176	

11.1 Definition of Characteristics.

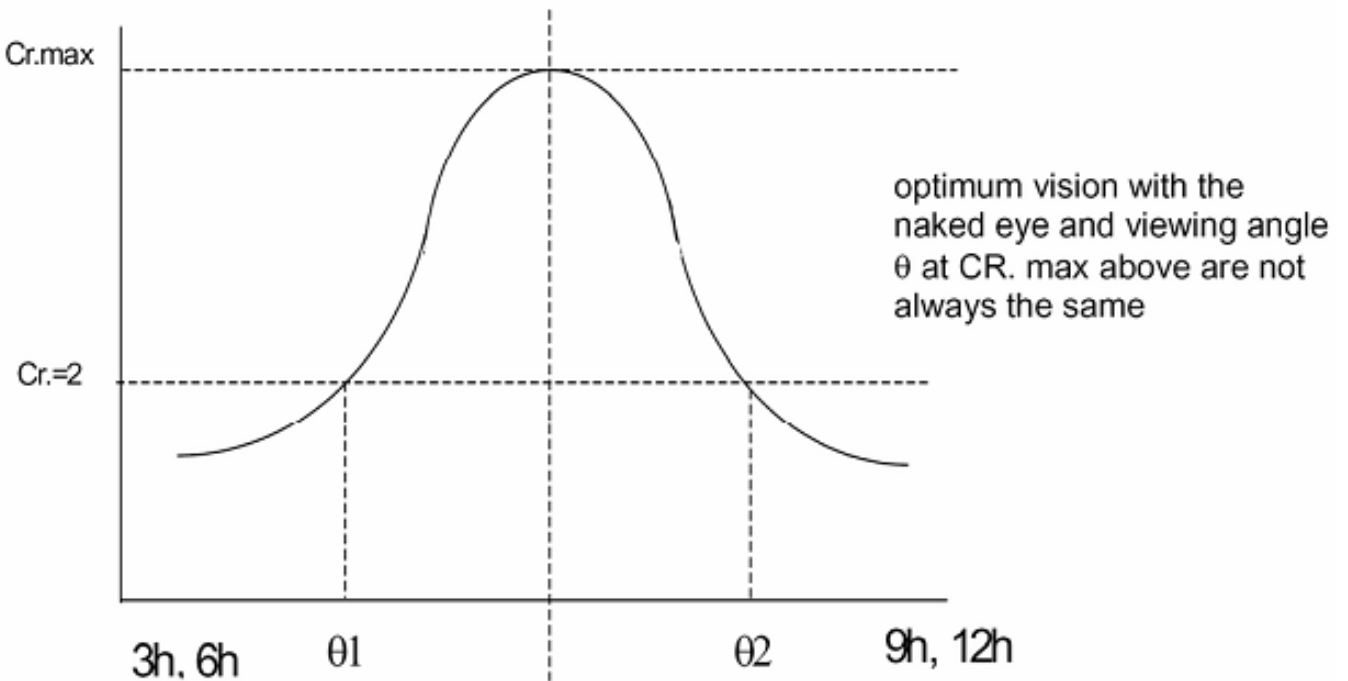


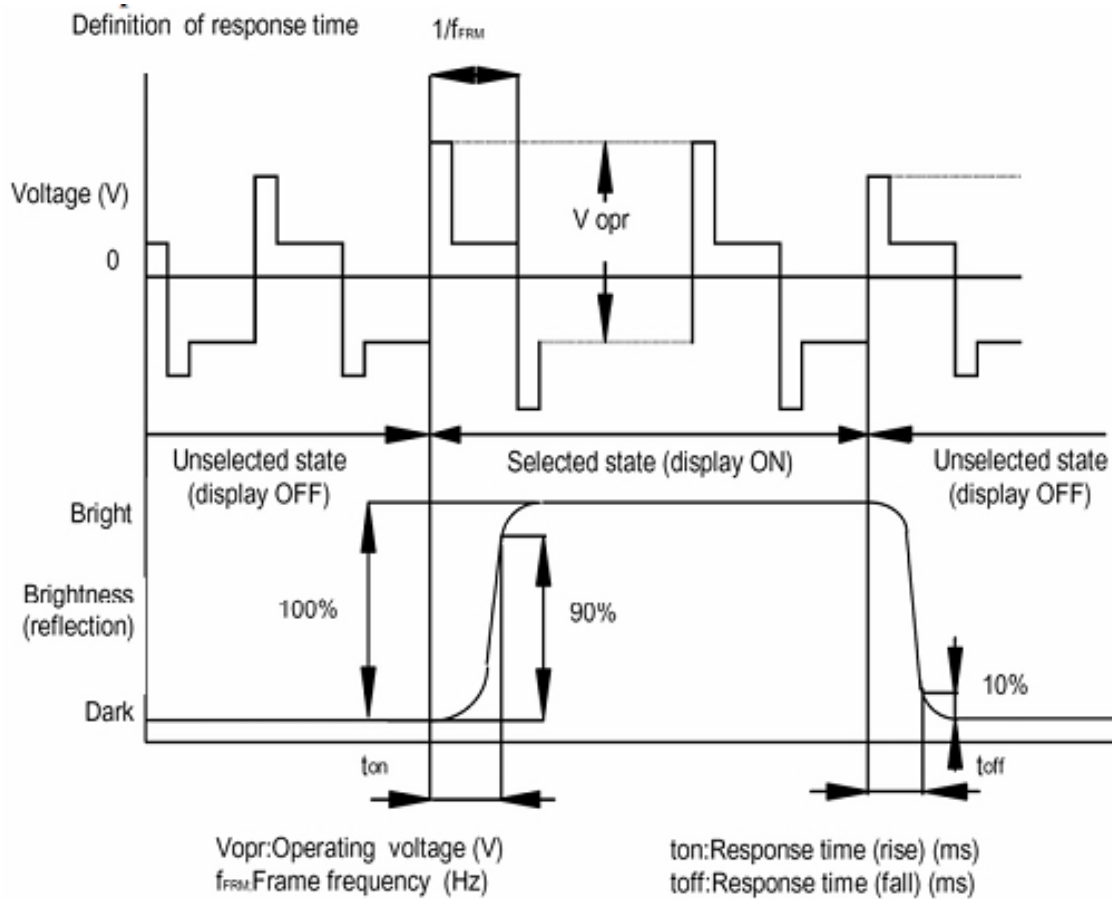
Definition of contrast  $Cr. = \frac{B2}{B1} = \frac{\text{Bright curve of not selected segment}}{\text{Bright curve of selected segment}}$



11.2 Definition of Viewing Angle

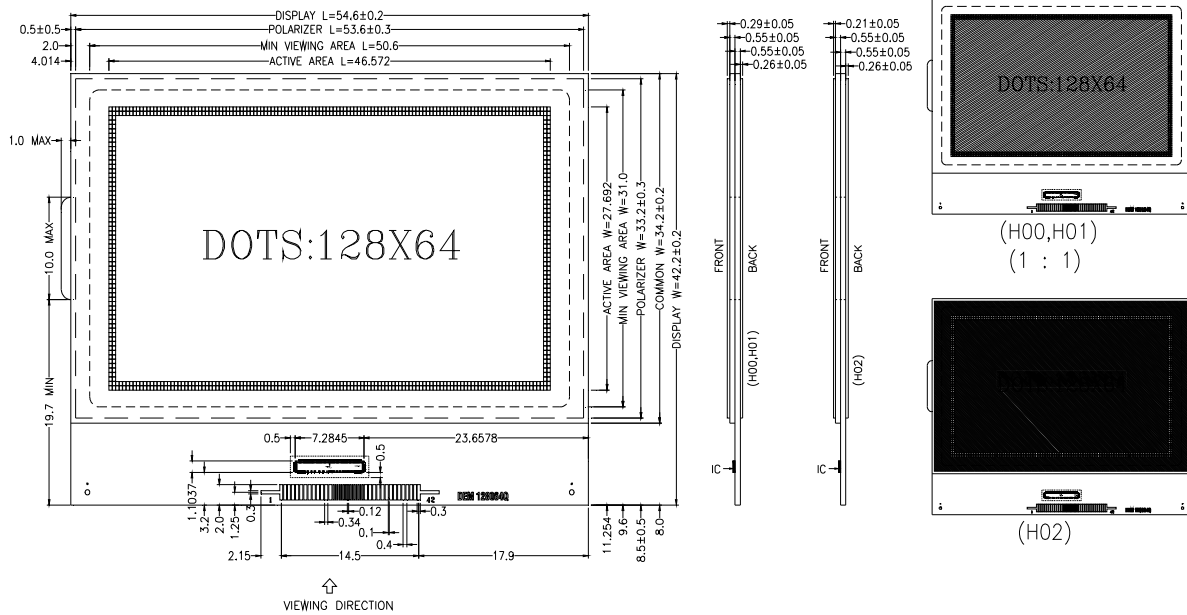
Definition of viewing angle  $\theta 1$  and  $\theta 2$





## 12. LCD ARTWORK

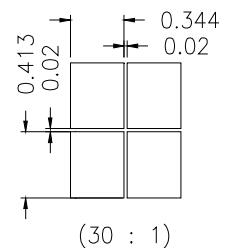
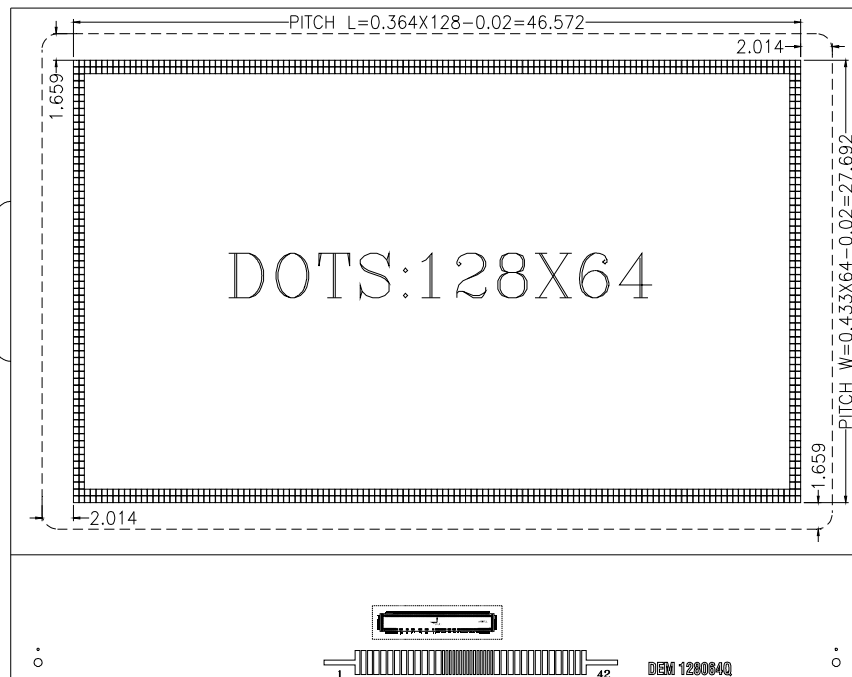
### 12-1 LCD ARTWORK



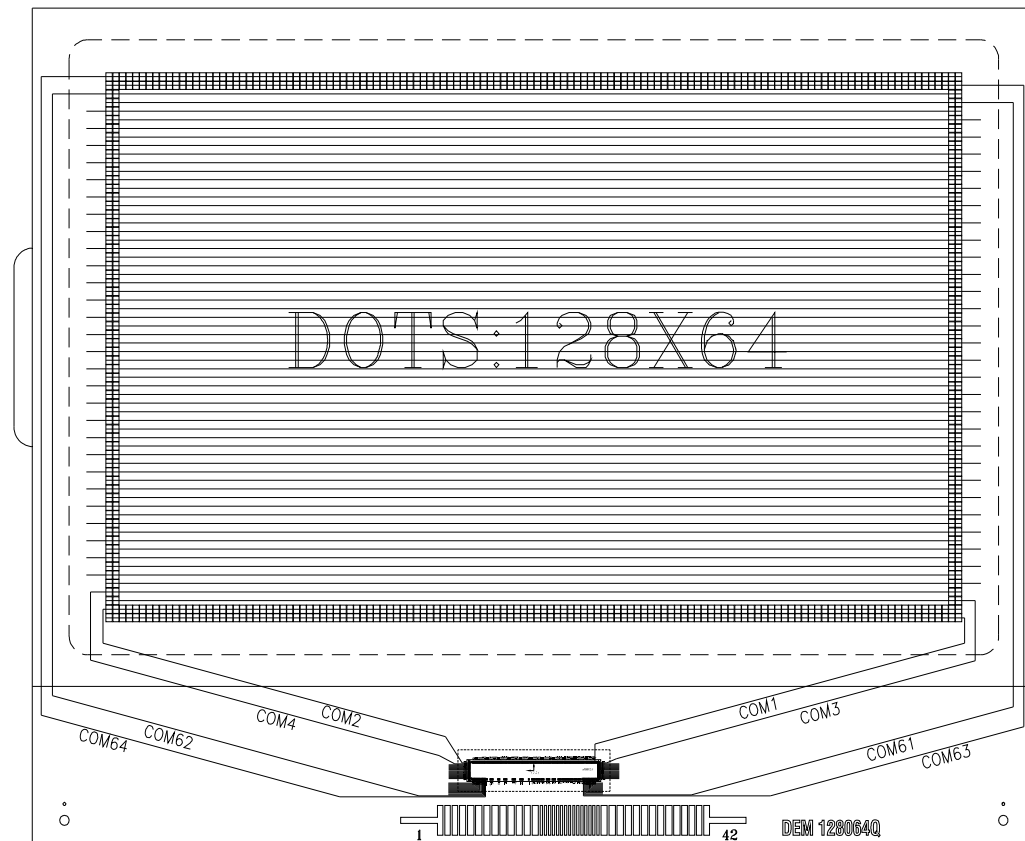
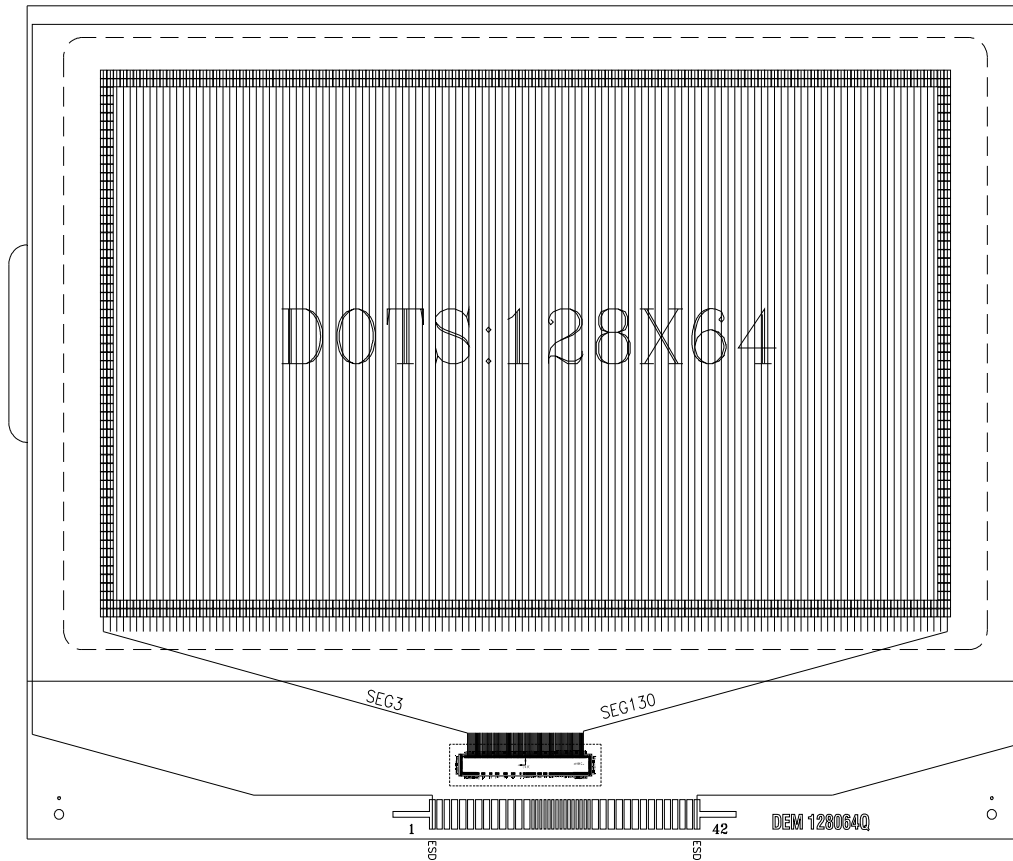
PIN Interface(LCD)

PIN	1	2~6	7	8	9	10	11	12	13	14	15	16	17	18
NAME	ESD	NC	VLCD	VB0+	VB0-	VB1-	VB1+	VSS	VDD	BM1	BM0	D7	D6	D5
PIN	19	20	21	22	23	24	25	26	27	28	29~41	42		
NAME	D4	D3	D2	D1	DO	WR1	WRO	CD	RST	CSO	NC	ESD		

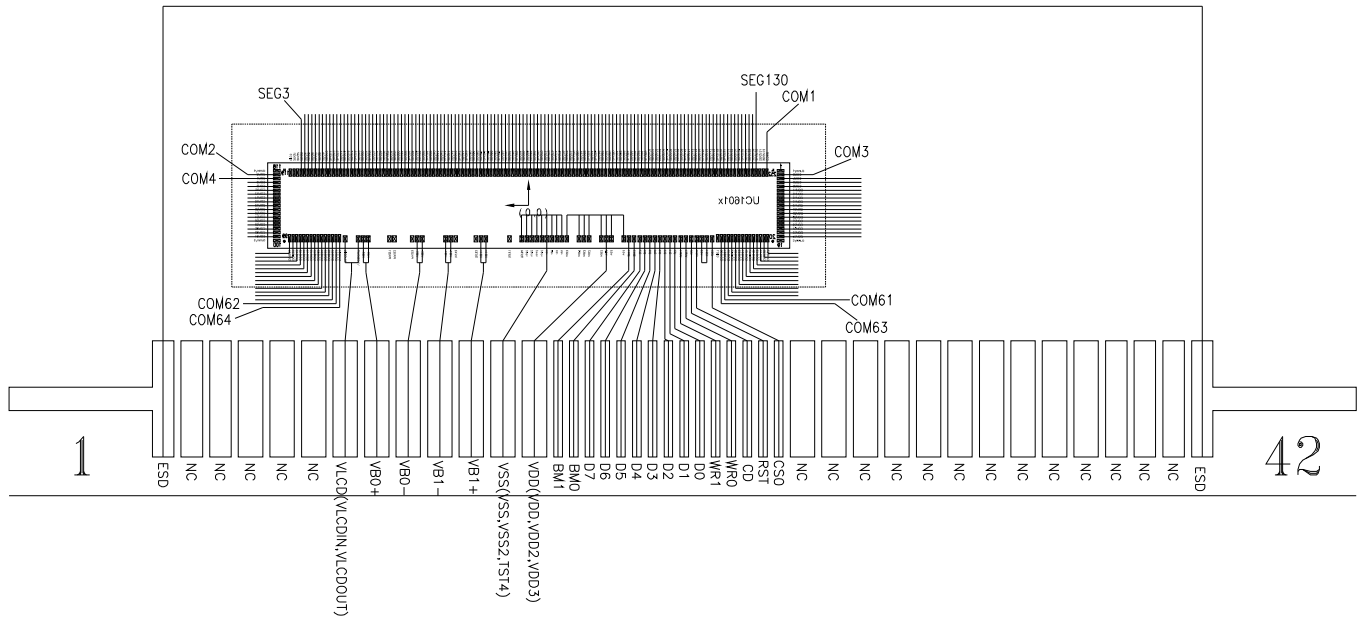
### 12-2 Labelling



12-3 SEG LAYOUT & COM LAYOUT



12-4. IC LAYOUT



13. ACCEPT QUALITY LEVEL (AQL)

Inspection Plan: ANSI Z-1.4, Normal Inspection Level II, Single Sampling Plan

14. RELIABILITY TEST

Operating life time: 50000 hours (at room temperature without direct irradiation of sunlight)

Reliability Characteristics shall meet following requirements.

Test Item	Test Condition
High Temperature Storage	+80°C x 96hrs
Low Temperature Storage	-30°C x 96hrs
High Temperature Operation	+70°C x 96hrs
Low Temperature Operation	-20°C x 96hrs
High Temperature, High Humidity	+70°C x 90%RH x 96hrs
Thermal Shock	-20°C x 30min → +25°C x 10s → +70°C x 30min 10Cycles
Vibration Test	Frequency x Swing x Time 40Hz x 4mm x 4hrs
Drop Test	Drop height x No. of drops 1.0m x 6drops

**15 LCD MODULES HANDLING PRECAUTIONS**

- Please remove the protection foil of polarizer before using.
- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.
- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.
- To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
  - Be sure to ground the body when handling the LCD module.
  - Tools required for assembly, such as soldering irons, must be properly grounded.
  - To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
  - The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.
- Storage precautions  
When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / 0°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

**16 OTHERS**

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.
- If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.
- To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules:
  - Exposed area of the printed circuit board
  - Terminal electrode sections