Display Elektronik GmbH

DATA SHEET

STANDARD OLED/PLED

DEP 128128D - W

Product Specification ***Version : 4***

09.05.2013

History of Version

Version	Contents	Date	Note
01	NEW VERSION	17.09.2009	SPEC.
02	Add contrast setting Modify seal color (white→black)	09.11.2011	
03	UPDATE Quality Assurance、Reliability ADD Precautions for Handling、Precautions for Electrical、Precautions for Storage	05.11.2012	
04	Modify	09.05.2013	

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1. General Specification

(1) Mechanical Dimension

Item	Standard Value	Unit
Number of dots	128x128	dots
Module dimension (L*W*H)	33.8*43.7*1.41(MAX)	mm
Active area	26.86*26.86	mm
Dot size	0.19(W)×0.19(H)	mm
Dot pitch	0.21(W)×0.21 (H)	mm
Color	White	

(2) Controller IC: SSD1327 Controller

(3) Temperature Range

Operating	-40 ~ +70℃
Storage	-40 ~ +85℃

2. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-40	—	+70	℃
Storage Temperature	TST	-40	—	+85	℃
Input Voltage	VI	0.3	—	4.0	V
Operating lifetime		10000(1)			Hrs
Operating lifetime		11000(2)			Hrs
Operating lifetime		12000(3)			Hrs

* Note:

(A) Under Vcc = 15V, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 100 cd/m^2:

- Contrast setting : 0x9b - Frame rate : 105Hz - Duty setting : 1/128

(2) Setting of 90 cd/m^2:

- Contrast setting : 0x77 - Frame rate : 105Hz - Duty setting : 1/128

(3) Setting of 80 cd/m2:

- Contrast setting : 0x60 - Frame rate : 105Hz - Duty setting : 1/128

3. Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage For Logic	V_{DD}-V_{SS}	—	2.6	3.3	3.5	V
Supply Voltage For Panel	Vcc-V_{SS}	—	14.5	15	15.5	V
Input High Vol	V_{IH}	—	0.8V_{DD}	—	V_{DD}	V
Input Low Vol	V_{IL}	—	0	—	0.2V_{DD}	V
Output High Vol	V_{OH}	—	0.9V_{DD}	—	V_{DD}	V
Output Low Vol.	V_{OL}	—	0	—	0.1V_{DD}	V
Supply Current (with built-in positive voltage)	I_{DD}	—	—	170	—	mA

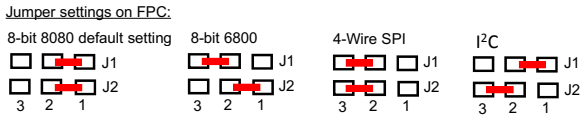
4. Optical Characteristics

Item	Min.	Typ.	Max.	Unit
View Angle	160	—	—	deg
Dark Room contrast	2000:1	—	—	—
Response Time	—	10	—	us

5. Interface Pin Function

Pin No.	Symbol	Level	Description
1	Vss	0V	Ground
2	Vdd	3.3V	Supply voltage for logic
3	CS	H/L	Chip select pin
4	/RES	H/L	Hardware Reset pin
5	D/C	H/L	H: Data; L: Command.
6	WR	H/L	write signal pin
7	RD	H/L	Read signal pin
8	DB0	H/L	Data bus line
9	DB1	H/L	Data bus line
10	DB2	H/L	Data bus line
11	DB3	H/L	Data bus line
12	DB4	H/L	Data bus line
13	DB5	H/L	Data bus line
14	DB6	H/L	Data bus line
15	DB7	H/L	Data bus line
16	DISPOFF/ VCC	H/L H	DISF: VCC Voltage ON/OFF VCC: Supply Voltage For OLED

Default: Parallel 8-Bit 8080 Interface
68j : Parallel 8-Bit 6800 Interface Special Code
20i : SPI Interface Special Code
20a: I2C Interface Special Code

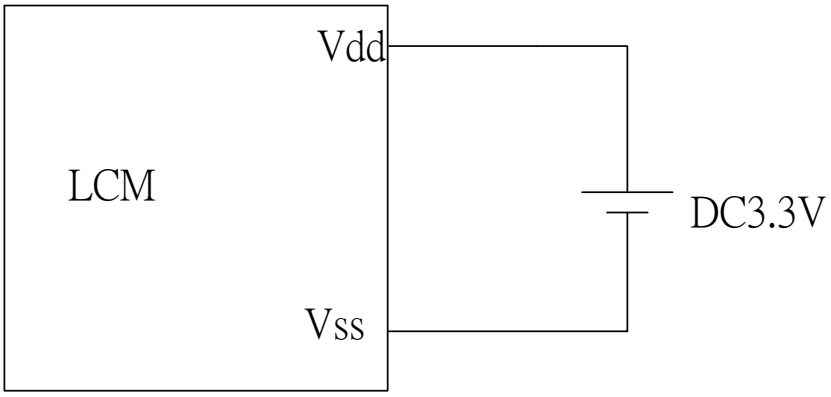


MCU interface assignment under different bus interface mode

Pin Name / Bus Interface	Data/Command Interface								Control Signal				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
4-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	D/C#	RES#
I^2C	Tie LOW					SDA_{OUT}	SDA_{IN}	SCL	Tie LOW			SA0	RES#

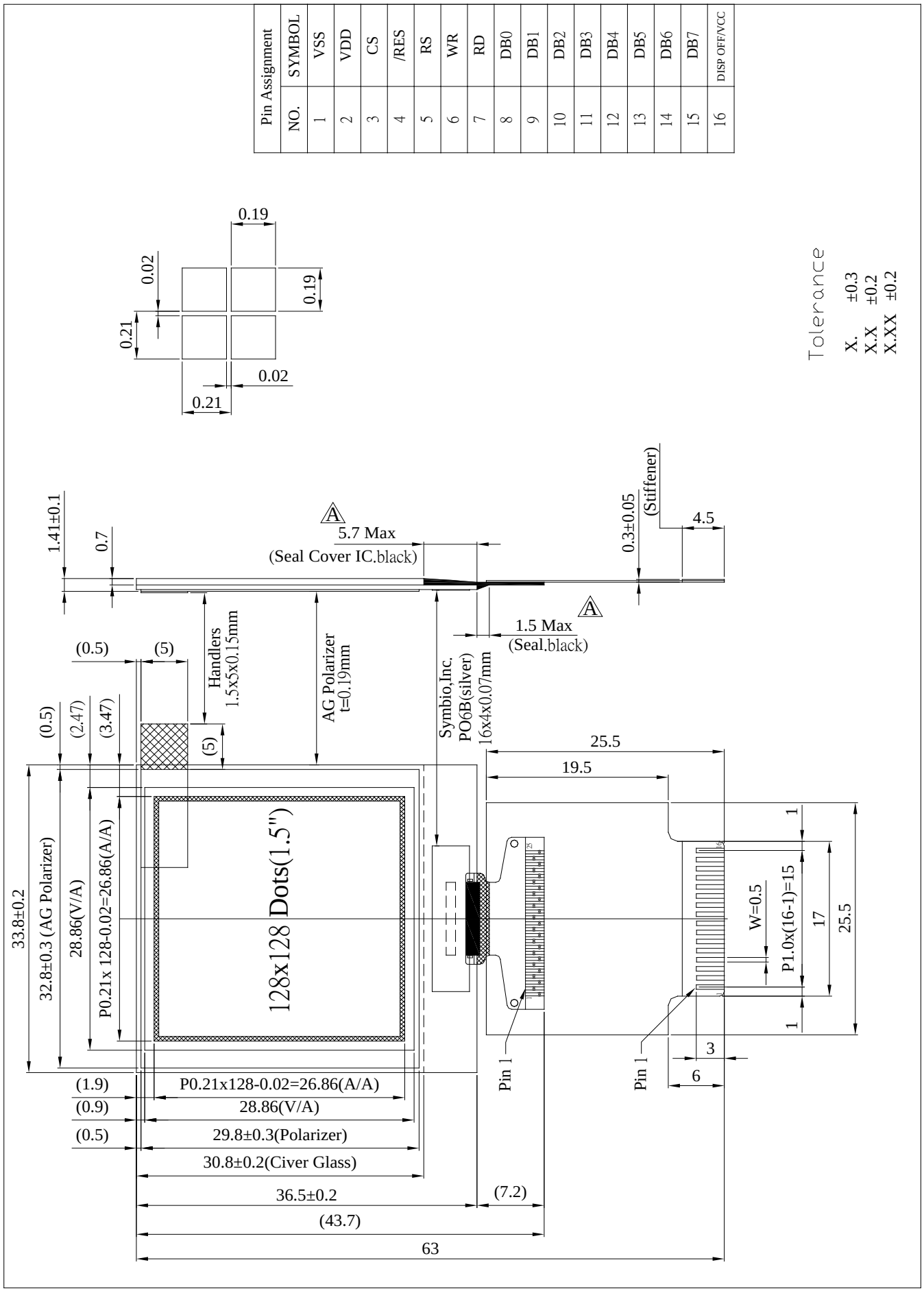
6. Power supply for LCD Module

LCM operating on "DC 3.3V " input with built-in positive voltage



7. Drawing

Pin Assignment	
NO.	SYMBOL
1	VSS
2	VDD
3	CS
4	/RES
5	RS
6	WR
7	RD
8	DB0
9	DB1
10	DB2
11	DB3
12	DB4
13	DB5
14	DB6
15	DB7
16	DISP OFF/VCC



8. SSD1327 controller data

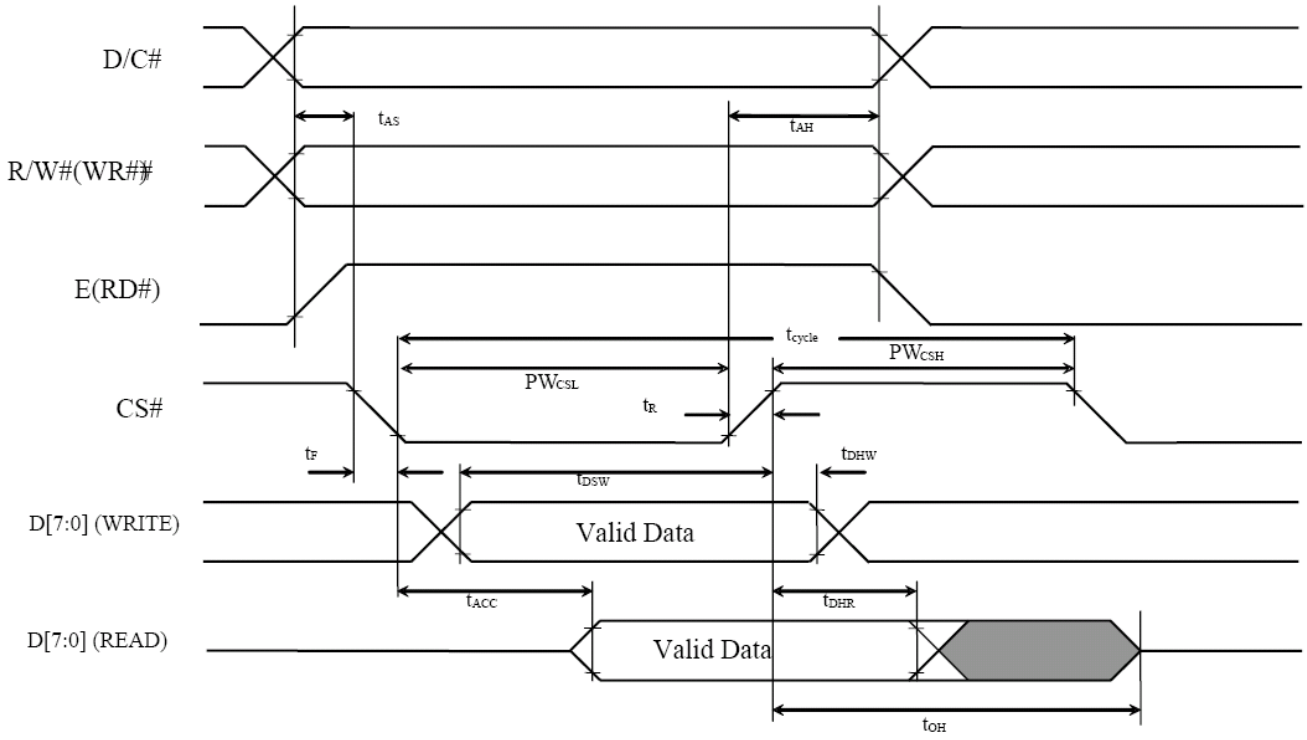
8.1 Timing Characteristics

6800 MPU Interface

(V_{CI} - V_{SS} = 1.65V to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

6800-series MCU parallel interface characteristics



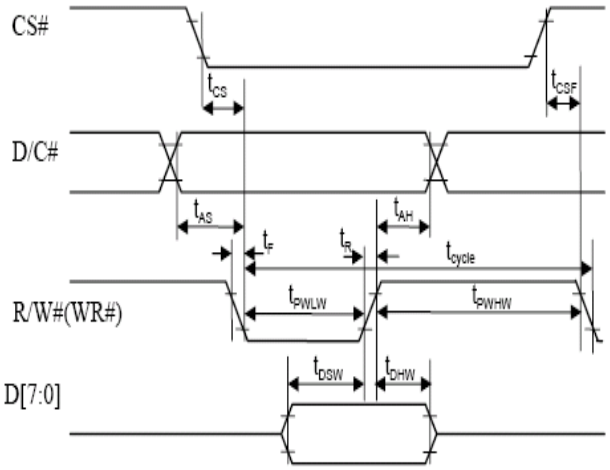
8080 MPU Interface

(V_{CI} - V_{SS} = 1.65V to 3.5V, T_A = 25°C)

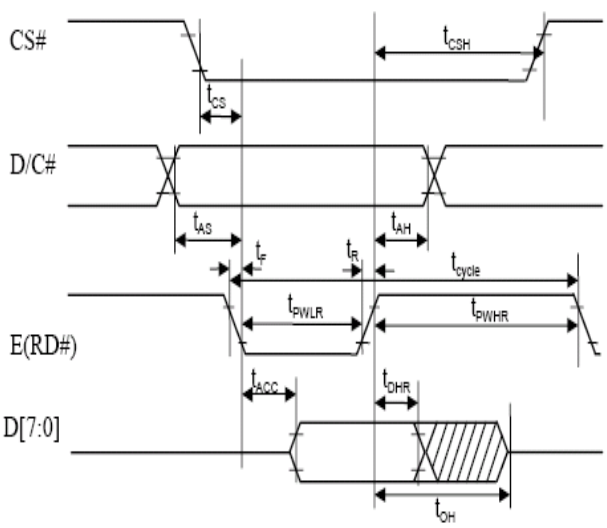
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series MCU parallel interface characteristics

Write cycle



Read cycle



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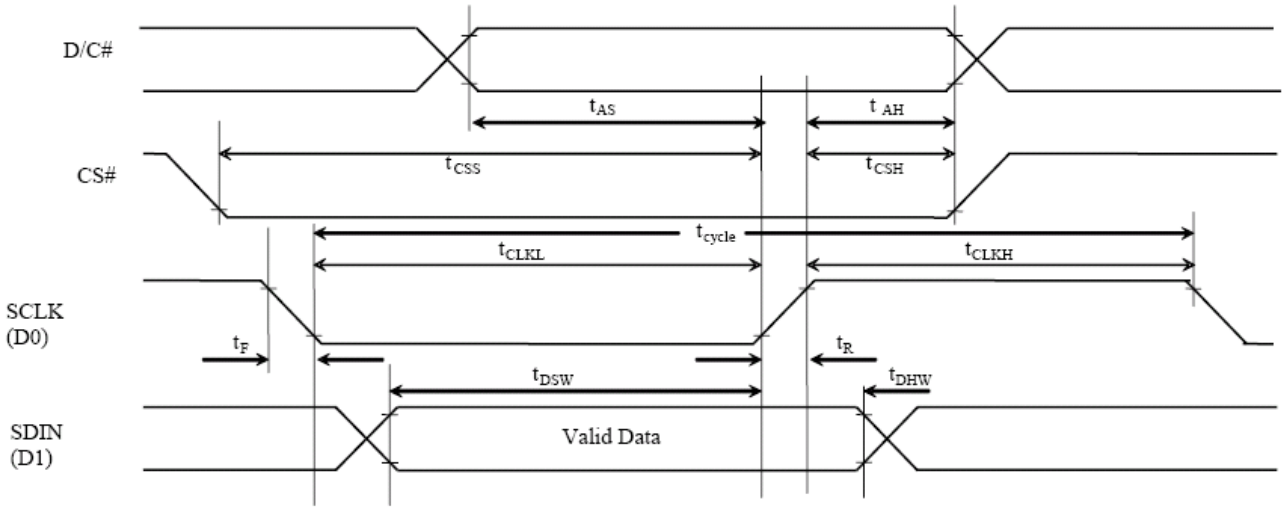
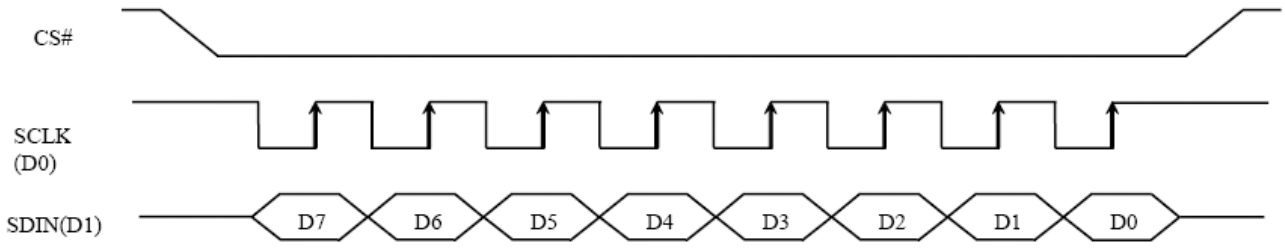
Serial Interface

(V_{CI} - V_{SS} = 1.65V to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Serial interface characteristics (4-wire SPI)



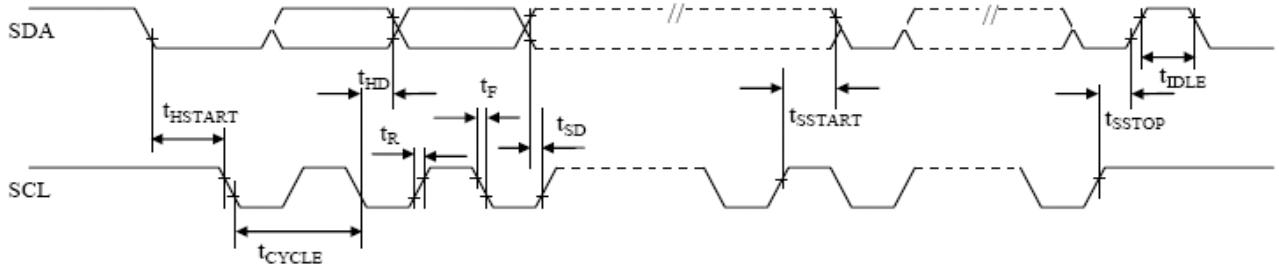


I2C Interface

(V_{CI} - V_{SS} = 1.65V to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

I^2C interface Timing characteristics



8.2 Display Control Instruction

(R/W#(WR#) = 0, E(RD#) = 1 unless specific setting is stated)

1. Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0 0	15 A[5:0] B[5:0]	0 * *	0 * *	0 A_5 A_5	1 A_4 A_4	0 A_3 A_3	1 A_2 A_2	0 A_1 A_1	1 A_0 A_0	Set Column Address	Setup Column start and end address A[5:0]: Start Address, range:00h~3Fh, (RESET = 00h) B[5:0]: End Address, range:00h~3Fh, (RESET = 3Fh)
0 0 0	75 A[6:0] B[6:0]	0 * *	0 A_6 A_6	0 A_5 A_5	1 A_4 A_4	0 A_3 A_3	1 A_2 A_2	0 A_1 A_1	1 A_0 A_0	Set Row Address	Setup Row start and end address A[6:0]: Start Address, range:00h~7Fh, (RESET = 00h) B[6:0]: End Address, range:00h~7Fh, (RESET = 7Fh)
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Control	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 7Fh)
0	84 ~ 86	1	0	0	0	0	1	X_1	X_0	Reserved	Command for no operation
0 0	A0 A[7:0]	1 0	0 A_6	1 0	0 A_4	0 0	0 A_2	0 A_1	0 A_0	Set Re-map	Re-map setting in Graphic Display Data RAM (GDDRAM) A[0] = 0b, Disable Column Address Re-map (RESET) A[0] = 1b, Enable Column Address Re-map A[1] = 0b, Disable Nibble Re-map (RESET) A[1] = 1b, Enable Nibble Re-map A[2] = 0b, Enable Horizontal Address Increment (RESET) A[2] = 1b, Enable Vertical Address Increment A[3] = 0b, Reserved (RESET) A[4] = 0b, Disable COM Re-map (RESET) A[4] = 1b, Enable COM Re-map A[5] = 0b, Reserved (RESET) A[6] = 0b, Disable COM Split Odd Even (RESET) A[6] = 1b, Enable COM Split Odd Even A[7] = 0b, Reserved (RESET)
0 0	A1 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	A[6:0]: Vertical shift by setting the starting address of display RAM from 0 ~ 127 (RESET = 00h)

1. Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0	A2 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	A[6:0]: Set vertical offset by COM from 0 ~ 127 (RESET = 00h) e.g. Set A[6:0] to 010000b to move COM16 towards COM0 direction for 16 row
0	A4 ~ A7	1	0	1	0	0	1	X_1	X_0	Set Display Mode	A4h = Normal display (RESET) A5h = All ON (All pixels have gray scale of 15, GS15) A6h = All OFF (All pixels have gray scale of 0, GS0) A7h = Inverse Display (GS0 → GS15, GS1 → GS14, GS2 → GS13, …)
0 0	A8 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set MUX Ratio	A[6:0]: Set MUX ratio from 16MUX ~ 128MUX: A[6:0] = 15 represents 16MUX A[6:0] = 16 represents 17MUX : A[6:0] = 126 represents 127MUX A[6:0] = 127 represents 128MUX (RESET) It should be noted that A[6:0]=0~14 is not allowed
0 0	AB A[0]	1 0	0 0	1 0	0 0	1 0	0 0	1 0	1 A_0	Function Selection A	A[0]=0b, Select external V_{DD} (i.e. Disable internal V_{DD} regulator) A[0]=1b, Enable internal V_{DD} regulator (RESET)
0	AE / AF	1	0	1	0	1	1	1	A_0	Set Display ON/OFF	A[0] = 0b, AEh = Display OFF (sleep mode) (RESET) A[0] = 1b, AFh = Display ON in normal mode
0 0	B1 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Phase Length	A[3:0]: Phase 1 period of 1~15 DCLK's e.g. A[3:0] = 1111b, 15 DCLK Clock (RESET = 0100b) A[7:4]: Phase 2 period of 1~15 DCLK's e.g. A[7:4] = 1111b, 15 DCLK Clocks (RESET = 0111b) **Note** (1) 0 DCLK is invalid in phase 1 & phase 2 (2) GS15 level pulse width must be set larger than the period of phase 1 + phase 2
0	B2	1	0	1	1	0	0	1	0	NOP	Command for no operation

1. Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0	B3 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Front Clock Divider /Oscillator Frequency	A[3:0]: Define divide ratio (D) of display clock (DCLK) Divide ratio=A[3:0]+1 (RESET is 0000b, i.e. divide ratio = 1) A[7:4]: Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. (Range:0000b~1111b) (RESET = 0000b)
0 0	B5 A[1:0]	1 0	0 0	1 0	1 0	0 0	1 0	0 A_1	1 A_0	GPIO	A[1:0] = 00b represents GPIO pin HiZ, input disable (always read as low) A[1:0] = 01b represents GPIO pin HiZ, input enable A[1:0] = 10b represents GPIO pin output Low (RESET) A[1:0] = 11b represents GPIO pin output High
0 0	B6 A[3:0]	1 *	0 *	1 *	1 *	0 A_3	1 A_2	1 A_1	0 A_0	Set Second pre-charge Period	A[3:0]: Second Pre-charge period of 1~15 DCLK's e.g. A[3:0] = 1111b, 15 DCLK Clock (RESET = 0100b) **Note** (1) This command is used to adjust the second pre-charge period after enabling the second pre-charge by setting A[1] = 1b in command D5h
0 0 0 … … … 0 0	B8 A1[5:0] A2[5:0] … … … A14[5:0] A15[5:0]	1 * * … … … * *	0 * * … … … * *	1 $A1_5$ $A2_5$ … … … $A14_5$ $A15_5$	1 $A1_4$ $A2_4$ … … … $A14_4$ $A15_4$	1 $A1_3$ $A2_3$ … … … $A14_3$ $A15_3$	0 $A1_2$ $A2_2$ … … … $A14_2$ $A15_2$	0 $A1_1$ $A2_1$ … … … $A14_1$ $A15_1$	0 $A1_0$ $A2_0$ … … … $A14_0$ $A15_0$	Set Gray Scale Table	The next 15 data bytes set the gray scale pulse width in unit of DCLK's. A1[5:0], value for GS1 level Pulse width A2[5:0], value for GS2 level Pulse width … A14[5:0], value for GS14 level Pulse width A15[5:0], value for GS15 level Pulse width **Note** (1) The pulse width value of GS1, GS2, ... , GS15 should not be equal. i.e. 0<GS1<GS2 … <GS15 (2) GS15 level pulse width must be set larger than the period of phase 1 + phase 2
0	B9	1	0	1	1	1	0	0	1	Linear LUT	The default Linear Gray Scale table is set in unit of DCLK's as follow GS0 level pulse width = 0; GS1 level pulse width = 0; GS2 level pulse width = 2; GS3 level pulse width = 4; : : GS14 level pulse width = 26; GS15 level pulse width = 28

1. Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	BB	1	0	1	1	1	0	1	1	NOP	Command for no operation
0 0	BC A[3:0]	1 0	0 0	1 0	1 0	1 A_3	1 A_2	0 A_1	0 A_0	Set Pre-charge voltage	Set pre-charge voltage level. A[3:0] | Hex code | Pre-charge voltage 0000 | 00h | 0.20 x V_{CC} : | : | : 0101 | 05h | 0.5 x V_{CC} (RESET) : | : | : 0111 | 07h | 0.613 x V_{CC} 1xxx | 08h | V_{COMH}
0 0	BE A[2:0]	1 0	0 0	1 0	1 0	1 0	1 A_2	1 A_1	0 A_0	Set V_{COMH}	Set COM deselect voltage level. A[2:0] | Hex code | V_{COMH} 000 | 00h | 0.72 x V_{CC} : | : | : 101 | 05h | 0.82 x V_{CC} (RESET) : | : | : 111 | 07h | 0.86 x V_{CC}
0 0	D5 A[2:0]	1 0	1 1	0 1	1 0	0 0	1 0	0 A_1	1 A_0	Function Selection B	A[1] = 0b: Disable second precharge (RESET) A[1] = 1b: Enable second precharge A[0] = 0b: Internal VSL (RESET) A[0] = 1b: Enable external VSL **Note** (1) Refer to Table 7-1 for VSL pin details
0 0	FD A[2]	1 0	1 0	1 0	1 1	1 0	1 A_2	0 1	1 0	Set Command Lock	A[2]: MCU protection status. A[2] = 0b, Unlock OLED driver IC MCU interface from entering command (RESET) A[2] = 1b, Lock OLED driver IC MCU interface from entering command **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command

2. Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	26 / 27	0	0	1	0	0	1	1	X_0	Continuous Horizontal Scroll Setup	26h, X[0]=0, Right Horizontal Scroll 27h, X[0]=1, Left Horizontal Scroll (Horizontal scroll by 1 column) A[7:0] : Dummy byte (Set as 00h) B[2:0] : Define start row address; range:00h~7Fh, (RESET = 00h) C[2:0] : Set time interval between each scroll step in terms of frame frequency 000b – 6 frames / 100b – 3 frames 001b – 32 frames / 101b – 4 frames 010b – 64 frames / 110b – 5 frame 011b – 256 frames / 111b – 2 frame D[2:0] : Define end row address; range:00h~7Fh, (RESET = 7Fh) The value of D[2:0] must be larger or equal to B[2:0] E[7:0] : Define start column address; range:00h~3Fh, (RESET = 00h) F[7:0] : Define end column address; range:00h~3Fh, (RESET = 3Fh) The value of F[2:0] must be larger or equal to E[2:0] G[7:0] : Dummy byte (Set as 00h)
0	A[7:0]	0	0	0	0	0	0	0	0		
0	B[6:0]	*	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	C[2:0]	*	*	*	0	0	C_2	C_1	C_0		
0	D[6:0]	*	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	E[5:0]	*	*	E_5	E_4	E_3	E_2	E_1	E_0		
0	F[5:0]	*	*	F_5	F_4	F_3	F_2	F_1	F_0		
0	G[7:0]	0	0	0	0	0	0	0	0		
0	2E	0	0	1	0	1	1	1	0	Deactivate scroll	Stop scrolling that is configured by command 26h/27h **Note** (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0	0	1	0	1	1	1	1	Activate scroll	Start scrolling that is configured by the scrolling setup commands :26h/27h with the following valid sequences: Valid command sequence 1: 26h ;2Fh. Valid command sequence 2: 27h ;2Fh.

Note
(1) "*" stands for "Don't care".

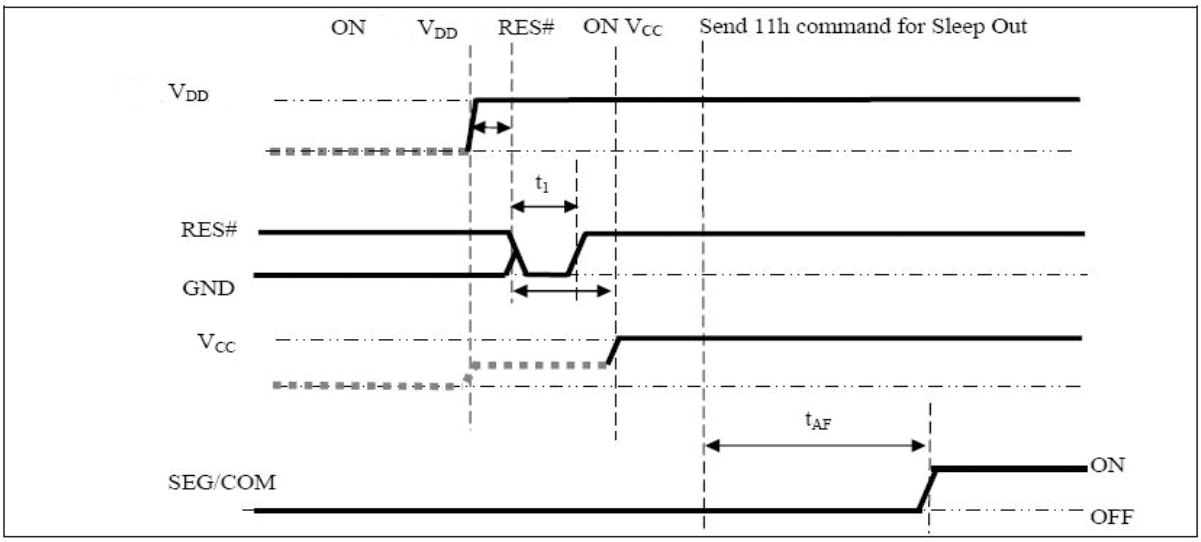
8.3 Power ON and OFF sequence

8.3.1 POWER ON / OFF SEQUENCE

The following figures illustrate the recommended power ON and power OFF sequence of SSD1351 (assume VCI and VDDIO are at the same voltage level and internal VDD is used).

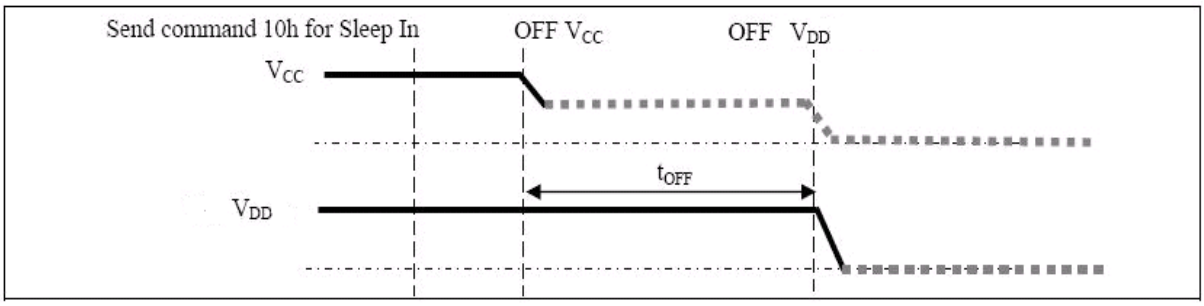
Power ON Sequence

1. Power ON VDD
2. After VDD become stable, set wait time at least 1ms (t0) for internal VDD become stable. Then set RES# pin LOW (logic low) for at least 2us (t1)(4) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 2us (t2). Then Power ON VCC. (1)
4. After VCC become stable, send command 11h for Sleep Out. SEG/COM will be ON after 200ms (tAF).



Power OFF Sequence

1. Send command AEh for display OFF.
2. Power OFF VCC. (1), (2)
3. Wait for tOFF. Power OFF VDD (where Minimum tOFF=80ms (3),Typical tOFF=100ms)



Note:

(1) Since an ESD protection circuit is connected between VCI,VDDIO and VCC,VCC becomes lower than VCI whenever VCI,VDDIO is ON and VCC is OFF as shown in the dotted line of VCC in above figures.
(2) VCC should be disabled when it is OFF.
(3) VCI, VDDIO should not be Power OFF before VCC Power OFF.
(4) The register values are reset after t1.
(5) Power pins(VDDIO, VCC) can never be pulled to ground under any circumstance.

9 Quality Assurance

9.1 Inspection conditions

1. The inspection and meaurement are performed under the following conditions,
2. unless otherwise specified.
3. Temperature: 25±5°C
4. Humidity: 50±10%R.H.
5. Distance between the panel and eyes of the inspector≧30cm

9.2 Inspection Parameters

Severity	Inspection Item	Defect	Remark
Major Defect	1. Panel	(1) Non-displaying	
		(2) Line defects	
		(3) Malfunction	
		(4) Glass cracked	
	2. Film	(1) Film dimension out of specification	Can not be assembled
	3. Dimension	(1) Outline dimension out of specification	
Minor Defect	1. Panel	(1) Glass scratch	Appearance defect
		(2) Glass cutting NG	
		(3) Glass chip	
	2. Polarizer	(1) Polarizer scratch	
		(2) Stains on surface	
		(3) Polarizer bubbles	
	3. Displaying	(1) Dim spot、Bright spot、dust	
	4. Film	(1) Damage (2) Foreign material	

<table>
<tr><th>Description</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>1. Glass scratch</td><td>
<table>
<tr><th>Width (mm)
W</th><th>Length (mm)
L</th><th>number of pieces permitted</th></tr>
<tr><td>W≦0.03</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td>0.03＜ W≦0.05</td><td>L≦3</td><td>3</td></tr>
<tr><td>0.05＜ W</td><td>------</td><td>None</td></tr>
<tr><td>beyond A.A.</td><td>------</td><td>Ignore</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>2. Polarizer bubble</td><td>
<table>
<tr><th>Size</th><th>number of pieces permitted</th></tr>
<tr><td>Φ≦0.2</td><td>Ignore</td></tr>
<tr><td>0.2＜Φ≦0.5</td><td>2</td></tr>
<tr><td>0.5＜Φ</td><td>0</td></tr>
<tr><td>beyond A.A.</td><td>Ignore</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>3. Dimming spot、
Lighting spot、
Dust</td><td>
<table>
<tr><th>average</th><th>number of</th></tr>
<tr><td>D ≦0.1</td><td>Ignore</td></tr>
<tr><td>0.1＜ D ≦0.15</td><td>2</td></tr>
<tr><td>0.15＜ D ≦0.2</td><td>1</td></tr>
<tr><td>0.2 ＜ D</td><td>0</td></tr>
<tr><td>beyond A.A.</td><td>Ignore</td></tr>
</table>
D=(long diameter + short diameter)/2.
Pixel off is not allowed.
</td><td>Minor</td></tr>
</table>

9.3 WARRANTY POLICY

We will provide one-year warranty for the products only if under specification operating conditions.
If there are functional defects found during the period of warranty, the defective products would be replaced on a one-to-one basis.
We would not be responsible for any direct/indirect liabilities consequential to any parties.

9.4 MTBF

9.4.1 .MTBF based on specific test condition is 10K hours.

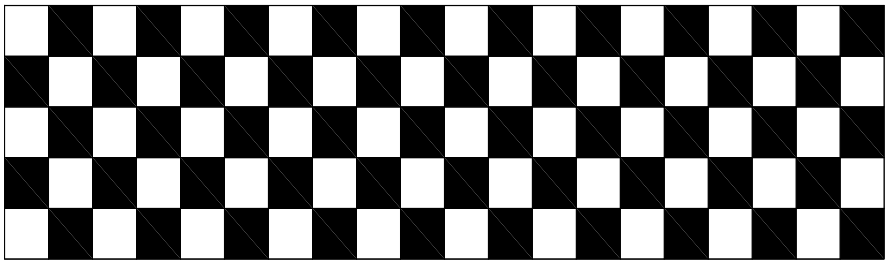
9.4.2 Test Condition:

9.4.2.1 Supply Voltage: Vcc=15V

9.4.2.2 Luminance: 100cd/m2

9.4.2.3 Operation temperature and humidity:25 ℃ and 50%RH

9.4.2.4 Run-Patterns:



9.4.3 Test Criteria:

Luminace has decayed to less than 50% of the initial measured luminance.

10.Reliability

■Content of Reliability Test

NO.	Items.	Specification	Applicable Standard
1	High temp. (Non-operation)	85°C, 240hrs	——
2	High temp. (Operation)	70°C, 120hrs	——
3	Low temp. (Operation)	-40°C, 120hrs	——
4	High temp. / High. humidity (Operation)	65°C, 90%RH, 120hrs	——
5	Thermal shock(Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles.	——
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	——

Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1 & 4 & 5.

Criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: >50% of initial value.
4. Current consumption : within ±50% of initial value.

Reliability Test

Only guarantees the reliability of the panel under the test conditions and durations listed in the specification, and is not responsible for any test results that are conducted using more stringent conditions and/or with lengthened durations. Also, when the testing the panel in a chamber or oven, make sure they won't produce any condensation on the panel, especially on the electrical leads, before lighting on the panel to see if it passes the test. Also the panel should rest for about an hour at room temperature and pressure before the measurement, as indicated in the specification. Be aware that one should use fresh panel for each of the reliability test items listed in the specification, in other words, don't use the panels that were tested for subsequent tests.